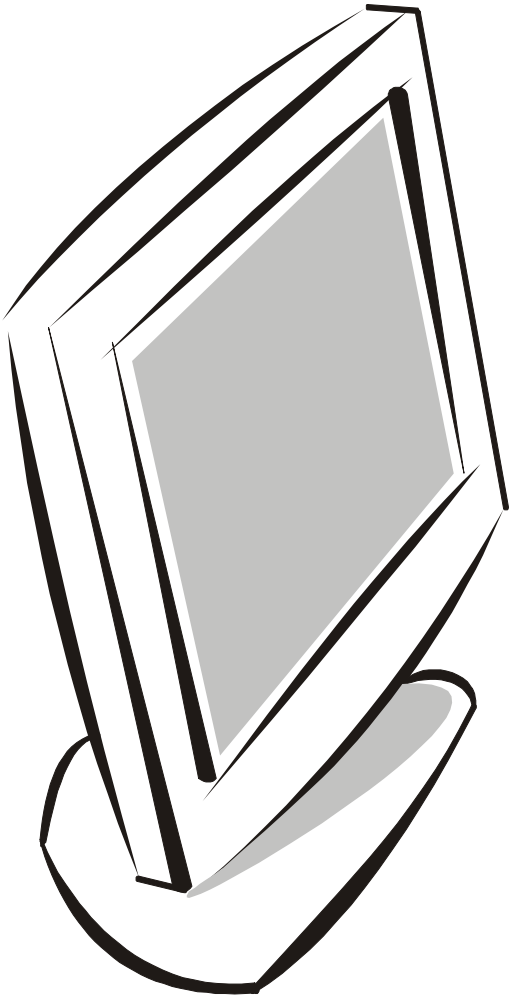
SERVICE MANUAL

SPECTRUM Series
LCD Monitor
LM-700/LM-700A



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P/N : 41A50-144

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MANUFACTURE DATA : JULY. 2001
REVISE 7 SEP 2001

TABLE OF CONTENTS

PAGE

1. SPECIFICATIONS FOR LCD MONITOR

1-1 General specifications

1. LCD-PANEL :
   Active display area 17 inches diagonal
   Pixel pitch 0.264 mm x 0.264 mm
   Pixel format 1280 x 1024 RGB vertical stripe arrangement

2. Display Color :
   8-bit, 16.7 million colors

3. ●External Controls :
   Power On/Off, Auto key, Left key, Right key (for 4-key)
   ●OSD menu Controls
   Contrast, Brightness, Focus, Clock,H-position, V-position, Language, Recall-7800, Recall-6500, Reset, Exit-osd, Red, Green, Blue, Selected Dos-resolution

4. Input Video Signal :
   Analog-signal 0.7Vpp
   Video signal termination impedance 75 OHM

5. Scanning Frequencies :
   Horizontal: 29 KHz - 80 KHz
   Vertical: 55 Hz – 75 Hz
   Pixel clock: 135 MHz

6. Factory Preset Timing : 18
   User Timings : 19
   Input signal tolerance : H tolerance ±1 K, V tolerance ±1 Hz

7. Power Source :
   Switching Mode Power Supply
   AC 100 – 240 V, 50/60 Hz Universal Type

8. Operating Temperature : 0℃ - 50℃ Ambient
   Non-operating Temperature : -20℃ - 60℃

9. Humidity :
   Operating : 20% to 80% RH (non-condensing)
   Non Operating : 5% to 95%RH (38.7℃ maximum wet bulb temperature)

10. Weight :
    5.5 kg
11. External Connection : 15Pin D-type Connector, AC power-Cord

12. View Angle : x-axis right/left = 60, y-axis up/down = 40 ,60

13. Outside dimension : Width x Height x Thickness = 422x 449 x 215 mm

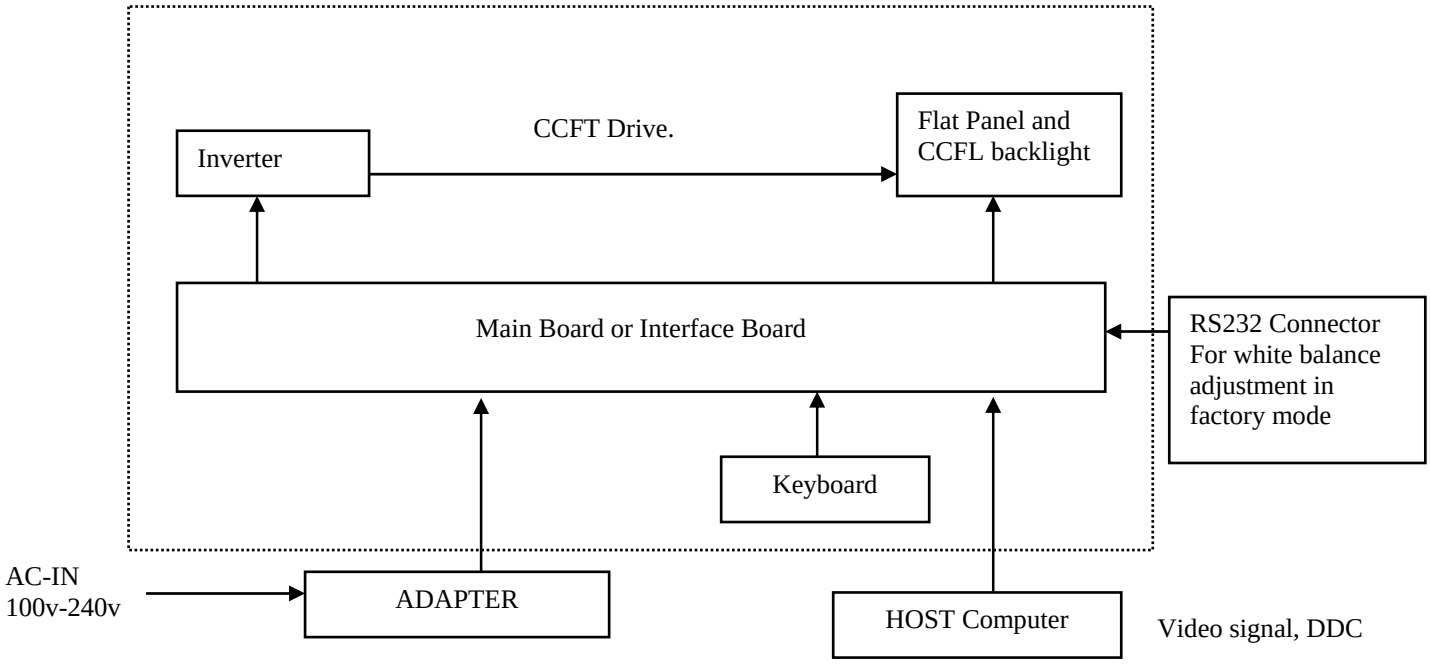
14. Plug and Play : VESA DDC1/DDC2B

15. Power saving : VESA DPMS

1-2 LCD MONITOR DESCRIPTION

The LCD MONITOR will contain an main board, an Inverter module, keyboard and External Adapter which house the flat panel control logic, brightness control logic, DDC and DC-DC conversion
The Inverter module will drive the backlight of panel .
The Adapter will provides the 12V DC-power 5 Amp to Main-board and Inverter module .

Monitor Block Diagram



1-3 Interface Connectors

(A) AC-Power Cable
(B) Video Signal Connectors and Cable
(C) External Adapter

2. PRECAUTIONS AND NOTICES

2-1 ASSEMBLY PRECAUTION

(1) Please do not press or scratch LCD panel surface with anything hard. And do not soil LCD panel surface by touching with bare hands (Polarizer film, surface of LCD panel is easy to be flawed)
In the LCD panel, the gap between two glass plates is kept perfectly even to maintain display characteristic and reliability. If this panel is subject to hard pressing, the following occurs :
(a) Uniform color (b) Orientation of liquid crystal becomes disorder
(2) Please wipe out LCD panel surface with absorbent cotton or soft cloth in case of it being soiled.
(3) Please wipe out drops of adhesive like saliva and water in LCD panel surface immediately.
They might damage to cause panel surface variation and color change.
(4) Do not apply any strong mechanical shock to the LCD panel.

2-2 OPERATING PRECAUTIONS

(1) Please be sure to unplug the power cord before remove the back-cover. (be sure the power is turn-off)
(2) Please do not change variable resistance settings in MAIN-BOARD, they are adjusted to the most suitable value. If they are changed, it might happen LUMINANCE does not satisfy the white balance spec.
(3) Please consider that LCD backlight takes longer time to become stable of radiation characteristic in low temperature than in room temperature.
(4) Please pay attention to displaying the same pattern for very long-time. Image might stick on LCD.

2-3 STORAGE PRECAUTIONS

(1) When you store LCD for a long time, it is recommended to keep the temperature between 0℃-40℃ without the exposure of sunlight and to keep the humidity less than 90% RH.
(2) Please do not leave the LCD in the environment of high humidity and high temperature such as 60℃ 90%RH.
(3) Please do not leave the LCD in the environment of low temperature; below -15℃.

2-4 HIGH VOLTAGE WARNING

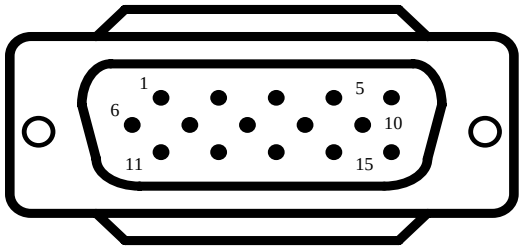
The high voltage was only generated by INVERTER module, if carelessly contacted the transformer on this module, can cause a serious shock. (the lamp voltage after stable around 600V, with lamp current around 8mA, and the lamp starting voltage was around 1500V, at Ta=25℃)

3. OPERATING INSTRUCTIONS

This procedure gives you instructions for installing and using the LM700 LCD monitor display.

1. Position the display on the desired operation and plug–in the power cord into External Adapter AC outlet. Three-wire power cord must be shielded and is provided as a safety precaution as it connects the chassis and cabinet to the electrical conduct ground. If the AC outlet in your location does not have provisions for the grounded type plug, the installer should attach the proper adapter to ensure a safe ground potential.

2. Connect the 15-pin color display shielded signal cable to your signal system device and lock both screws on the connector to ensure firm grounding. The connector information is as follow:



15 - Pin Color Display Signal Cable

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1.	RED	9.	5V power from VGA-card
2.	GREEN	10.	GND
3.	BLUE	11.	SYNC. GND
4.	GND	12.	SDA
5.	GND	13.	HORIZ. SYNC
6.	GND-R	14.	VERT. SYNC
7.	GND-G	15.	SCL
8.	GND-B		

3. Apply power to the display by turning the power switch to the "ON" position and allow about thirty seconds for Panel warm-up. The Power-On indicator lights when the display is on.
4. With proper signals feed to the display, a pattern or data should appear on the screen, adjust the brightness and contrast to the most pleasing display, or press auto-key to get the best picture-quality.
5. This monitor has power saving function following the VESA DPMS. Be sure to connect the signal cable to the PC.
6. If your LM700 LCD monitor requires service, it must be returned with the power cord & Adapter.

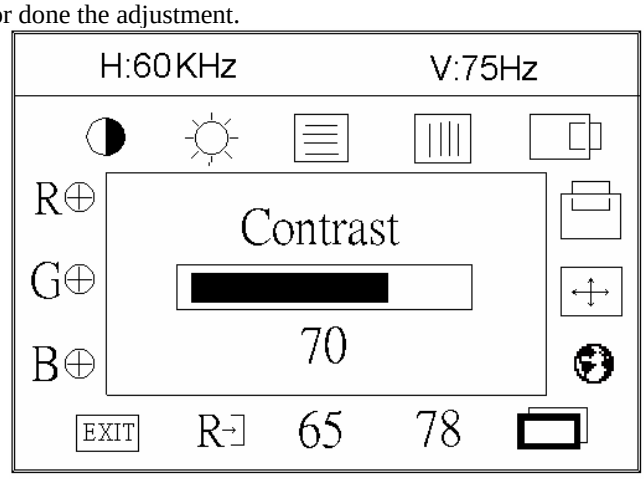
4. ADJUSTMENT

4-1 ADJUSTMENT CONDITIONS AND PRECAUTIONS

Adjustments should be undertaken only on following function : contrast, brightness focus, clock, h-position, v-position, red, green, blue since 6500 color & 7800 color.

4-2 ADJUSTMENT METHOD

Press MENU button to activate OSD Menu or make a confirmation on desired function, Press Left/Right button to select the function or done the adjustment.



1. White-Balance, Luminance adjustment
   Approximately 30 minutes should be allowed for warm up before proceeding white balance adjustment.

   Before started adjust white balance ,please setting the Chroma-7120 **MEM. Channel 5 to 7800** color and **MEM. channel 6 to 6500** color, (our 7800 parameter is x = 296 ±10, y = 311 ±10, Y = 160 ±5cd/m2 and 6500 parameter is x = 313 ±10, y = 329 ±10, Y = 160 ±5 cd/m^2)

   How to setting MEM.channel you can reference to chroma 7120 user guide or simple use " **SC**" key and " **NEXT**" key to modify xyY value and use "**ID**" key to modify the TEXT description

   Following is the procedure to do white-balance adjust

   Press MENU button during 2 seconds along with plug in the DC-power cord will activate the factory mode, and the OSD screen will located at **left top of panel**.

   I. Bias (Low luminance) adjustment :

   1. Press " AUTO" button , and wait for message " Pass" ,check the Blacklevel value on OSD should be large than 30, if less than 30 that means the offset calculation FAIL, please manual adjust the blacklevel to value 43
   2. set the contrast and brightness on OSD window to **maximal** value , RGB to "**50**"
   3. adjust the **VR501** on INTERFACE board until chroma 7120 measurement reach the value Y=240 cd/m^2 ±5 cd/m^2

   II. Gain adjustment :

   a. adjust 7800 color-temperature

   4. Set the Contrast of OSD function to 40, Brightness to 48
   5. Switch the chroma-7120 to **RGB-mode** (with press "MODE" button)
   6. switch the MEM.channel to Channel 05 (with up or down arrow on chroma 7120)
   7. The lcd-indicator on chroma 7120 will show x = 296 ±10, y = 311 ±10, Y = 160 ±5 cd/m^2
   8. Adjust the RED on OSD window until chroma 7120 indicator reached the value R=100

9. adjust the GREEN on OSD, until chroma 7120 indicator reached G=100
10. adjust the BLUE on OSD, until chroma 7120 indicator reached B=100
11. repeat above procedure (item 8,9,10) until chroma 7120 RGB value meet the tolence =100±2
12. switch the chroma-7120 to **xyY mod**e With press "MODE" button
13. Adjust the Contrast on OSD window until the Y measurement on chroma 7120 reached the value Y= 180 cd/m^2
14. Press 78 on OSD window to save the adjustment result

b. adjust 6500 color-temperature

1 Set the Contrast of OSD function to 40, Brightness to 48
2 Switch the chroma-7120 to **RGB-mode** (with press "MODE" button)
3 switch the MEM.channel to Channel 06 (with up or down arrow on chroma 7120)
4 The lcd-indicator on chroma 7120 will show x = 313 ±10, y = 329 ±10, Y = 160 ±5 cd/m^2
5 Adjust the RED on OSD window until chroma 7120 indicator reached the value R=100
6 adjust the GREEN on OSD, until chroma 7120 indicator reached G=100
7 adjust the BLUE on OSD, until chroma 7120 indicator reached B=100
8 repeat above procedure (item 5,6,7) until chroma 7120 RGB value meet the tolence =100 ±2
9 switch the chroma-7120 to **xyY mod**e With press "MODE" button
10 Adjust the Contrast on OSD window until the Y measurement on chroma 7120 reached the value Y= 180 cd/m^2
11 Press 65 on OSD window to save the adjustment result

Turn the POWER-button off to on to quit from factory mode (in USER-mode, the OSD window location was placed at middle of screen)

2. Clock adjustment
   Set the Chroma at pattern 63 (cross-talk pattern) or WIN98/95 shut-down mode (dot-pattern).
   Adjust until the vertical-Stripe-shadow as wide as possible or no visible.
   This function is adjust the PLL divider of ADC to generate an accurate pixel clock
   Example : Hsyn = 31.5KHz Pixel freq. = 25.175MHz (from VESA spec)
   The Divider number is (N) = (Pixel freq. x 1000)/Hsyn
   From this formula, we get the Divider number, if we fill this number in ADC register (divider register), the PLL of ADC will generate a clock which have same period with above Pixel freq.(25.175MHz) the accuracy of this clock will effect the size of screen.(this clock was called PIXEL-CLOCK)

3. Focus adjustment
   Set the Chroma at pattern 63 (cross talk pattern) or WIN98/95 shut down mode (dot-pattern).
   Adjust the horizontal interference as less as possible
   This function is adjust the phase shift of PIXEL-CLOCK to acquire the right pixel data .
   If the relationship of pixel data and pixel clock not so match, we will see the horizontal interference on screen ,we only find this phenomena in crosstalk pattern or dot pattern , other pattern the affect is very light

4. H/V-Position adjustment
   Set the Chroma to pattern 1 (crosshatch pattern) or WIN98/95 full-white pattern confirm above item 2 & 3 functions (clock & focus) was done well, if that 2 functions failed, the H/V position will be failed too.
   Adjust the four edge until all four-edges are visible at the edge of screen.

5. MULTI-LANGUAGE function
   There have 5 language for selection, press “MENU” to selected and confirm , press “ LEFT” or “ RIGHT” to change the kind of language (English , Deutch , Francais, Espanol, Italian)

6. Reset function
   Clear each old status of auto-configuration and re-do auto-configuration (for all mode)
   This function also recall 7800 color-temperature , if the monitor status was in “ Factory-mode” this reset function will clear Power-on counter (backlight counter) too.

7. OSD-LOCK function
   Press Left & Right key during switching on the monitor, the access to the OSD is locked, user only has access to “ Contrast, Brightness, Auto-key “.
   If the operator pressed the Left & Right during switching on the monitor again , the OSD is unlocked.

8. View Power-on counter and reset the Power-on counter(if not necessary , no suggest to entry factory mode)
   The Power-on counter was used to record how long the backlight of panel already working, the backlight life time was guarantee minimal 25000 hours, the maintainer can check the record only in factory mode.
   Press MENU button for 2 seconds along with plug-in DC power cord will be in factory mode, and the OSD screen will located at **left top of panel** but take cautions don’t press icon “78” & “65”, if you press 78/65 , your white-balance data will overlap with the new-one, and you must perform the white-balance process again.
   The result of counter was place at top of OSD, the maximal of record memory was 65000 hours, if exceed 65000 hours the counter will keep in 65000 hours until press “ RESET” at osd-menu in factory mode.
   The “ RESET” function in factory mode will execute following function:
   1. clear the Power-on counter to zero hours
   2. clear old auto-configuration status for all mode , so the monitor will automatically re-do auto-config when change to next mode or power on-off

4-3 FRONT PANEL CONTROL KNOBS

Power button : Press to switch on or switch off the monitor.
Auto button : to perform the automatic adjustment from CLOCK, FOCUS, H/V POSITION, but no affect the color-temperature
Left/Right button : select function or do an adjustment.
MENU button : to activate the OSD window or to confirm the desired function

5. CIRCUIT-DESCRIPTION

5-1 SPECIAL FUNCTION with PRESS-KEY

A). press **Menu** button during 2 seconds along with **plug-in the DC Power cord**:
That operation will set the monitor into "Factory- mode", in Factory mode we can do the White balance adjustment with RS232 , and view the Backlight counter (this counter is use to record the panel activate hours ,for convenient the maintainer to check the panel backlight life time)
In Factory mode, OSD-screen will locate in left top of screen.
Press POWER-button off to on once will quit from factory mode and back to user-mode.

B). Press **both Left & Right button along with Power button** off to on once will activate the OSD-LOCK function, repeat this procedure will disable OSD-LOCK
In OSD-LOCK function, all OSD function will be lock , except Contrast and Brighness

OSD-INDEX EXPLANATION

1. **CABLE NOT CONNECTED**: Signal-cable not connected.

2. **INPUT NOT SUPPORT**:
   a. INPUT frequency out of range: H > 81kHz, v > 75Hz or H < 28kHz, v < 55Hz
   b. INPUT frequency out of VESA-spec. (out of tolerance too far)

3. **UNSUPPORT mode, try different Video-card Setting**:
   Input frequency out of tolerance, but still can catch-up by our system (if this message show, that means, this is new-user mode, AUTO-CONFIG will disable)

5-2 THE Different on MAINBOARD or other ACCESSORY when using different PANEL type

1). The **MCU software** should be change
example : for CHI-MEI panel , the MCU part-number is 56A-1125-61-M
for Hyundai panel , the MCU part-number is 56A-1125-61-Y

and the other ACCESSORY when use different panel type should be change as following:

1). The **INVERTER** module for CHI-MEI panel part-number is 79AL17-1-S
for Hyundai panel the INVERTER part number is 79A-L17-3-S
2). The **cable to Panel side** for CHI-MEI panel part number is 95A8018-30-1
for HYUNDAI panel is 95A8018-30-3
3). The **Dsub cable** for CHI-MEI is 89A-174D-5BF-GLF,
for Hyundai is 89A-174-L17-3.
4). The **Mechanical accessory** is change or adding as follow;

	CHI-MEI PANEL M170E1	**Hyundai PANELHT17E11-100**
MAIN-FRAME	15A5684-1	15A5705-1
Panel	750ALCD170-3	750ALCD170-4

5-3 SIMPLE-INTRODUCTION about LM700 chipset

1. GMZAN1 (all-in-one chip solution for ADC, OSD, scalar and interpolation) :
   USE for computer graphics images to convert analog RGB data to digital data with interpolation process, zooming, generated the OSD font , perform overlay function and generate drive-timing for LCD-PANEL.

2. M6759 (ALI- MCU, type 8052 series with 64k Rom-size and 512 byte ram) :
   Use for calculate frequency, pixel-dot , detect change mode, rs232-communication, power-consumption control, OSD-index warning , …etc.

3. 24LC21 (MicroChip IC) :
   EePROM type, 1K ROM-SIZE, for saving DDC-CONTENT.

4. 24C04 (ATMEL IC) :
   EePROM type, 4K ROM-SIZE, for saving AUTO-config data, White-balance data, and Power-key status and Backlight-counter data.

5. LM2569S(NS brand switching regulator 12V to 5V with 3A load current) .

6. AIC 1084-33CM (AIC brand linear regulator 5V to 3.3V)

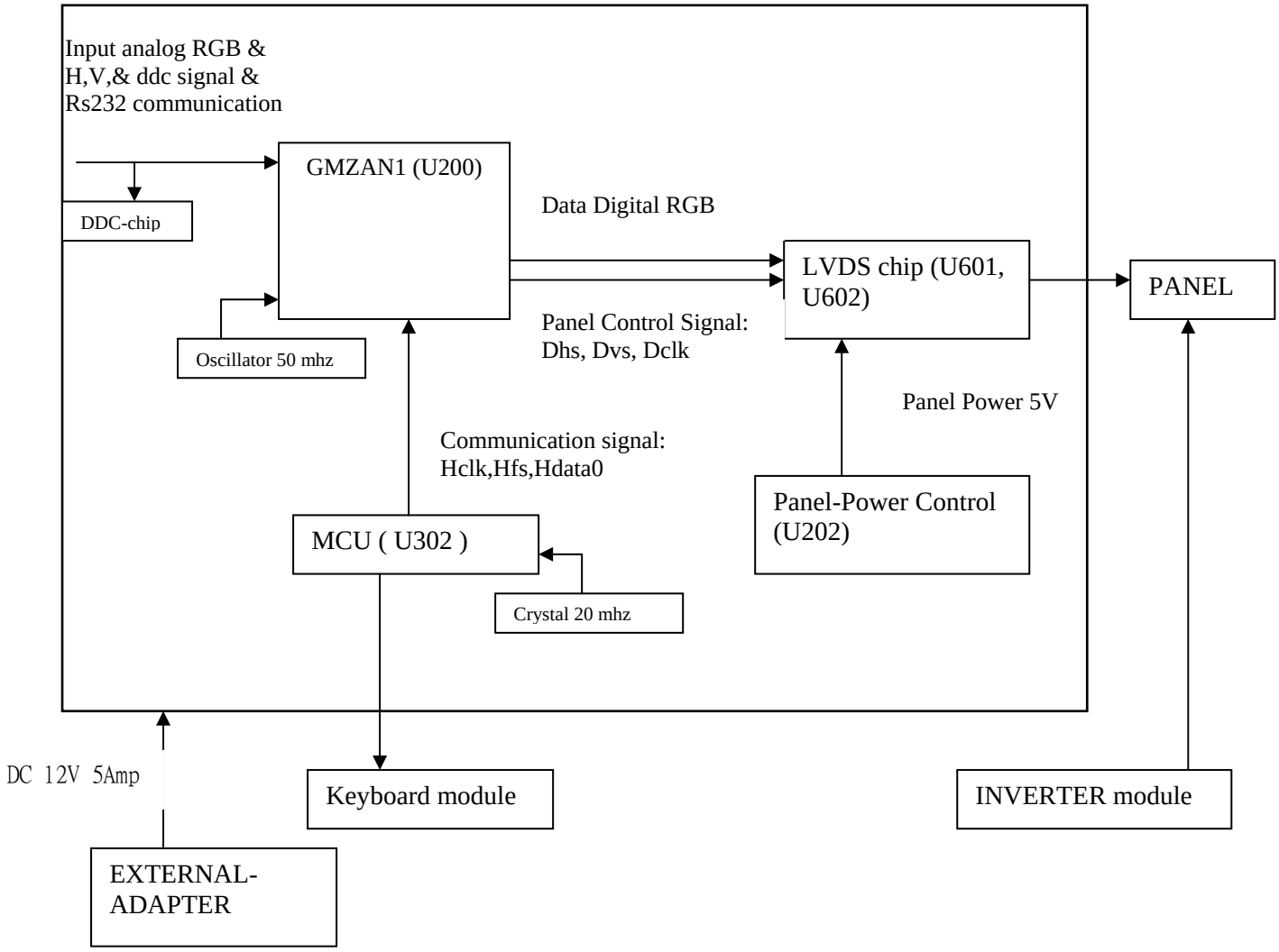
7. LVDS (use NOVATEK NT7181F)
   Convert the TTL signal to LVDS signal
   The advantage of LVDS signal is : the wire can be lengthen and eliminate wire number , low EMI .
   LVDS signal is high frequency but low voltage, only 0.35 VPP ,the frequency is seven times higher than TTL

MODULE-TPYE COMPONENT :

1. ADAPTER : CONVERSION-module to convert AC 110V-240V to 12VDC, with 5.0 AMP

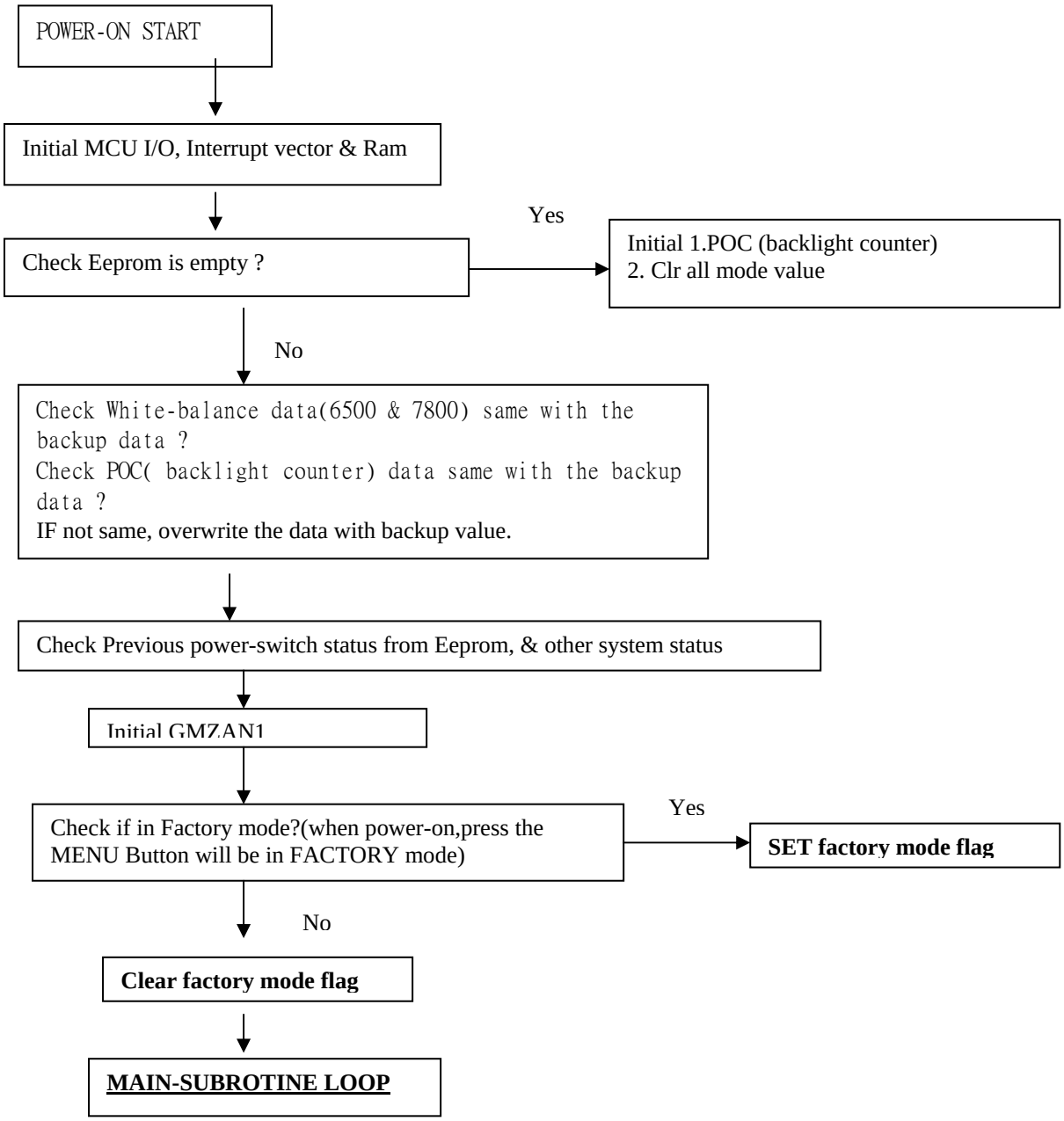
2. INVERTER : CONVERSION-module to convert DC 12V to High-Voltage around 1600V, with frequency 30K-80Khz, 7mA-9Ma

Main-board Block diagram

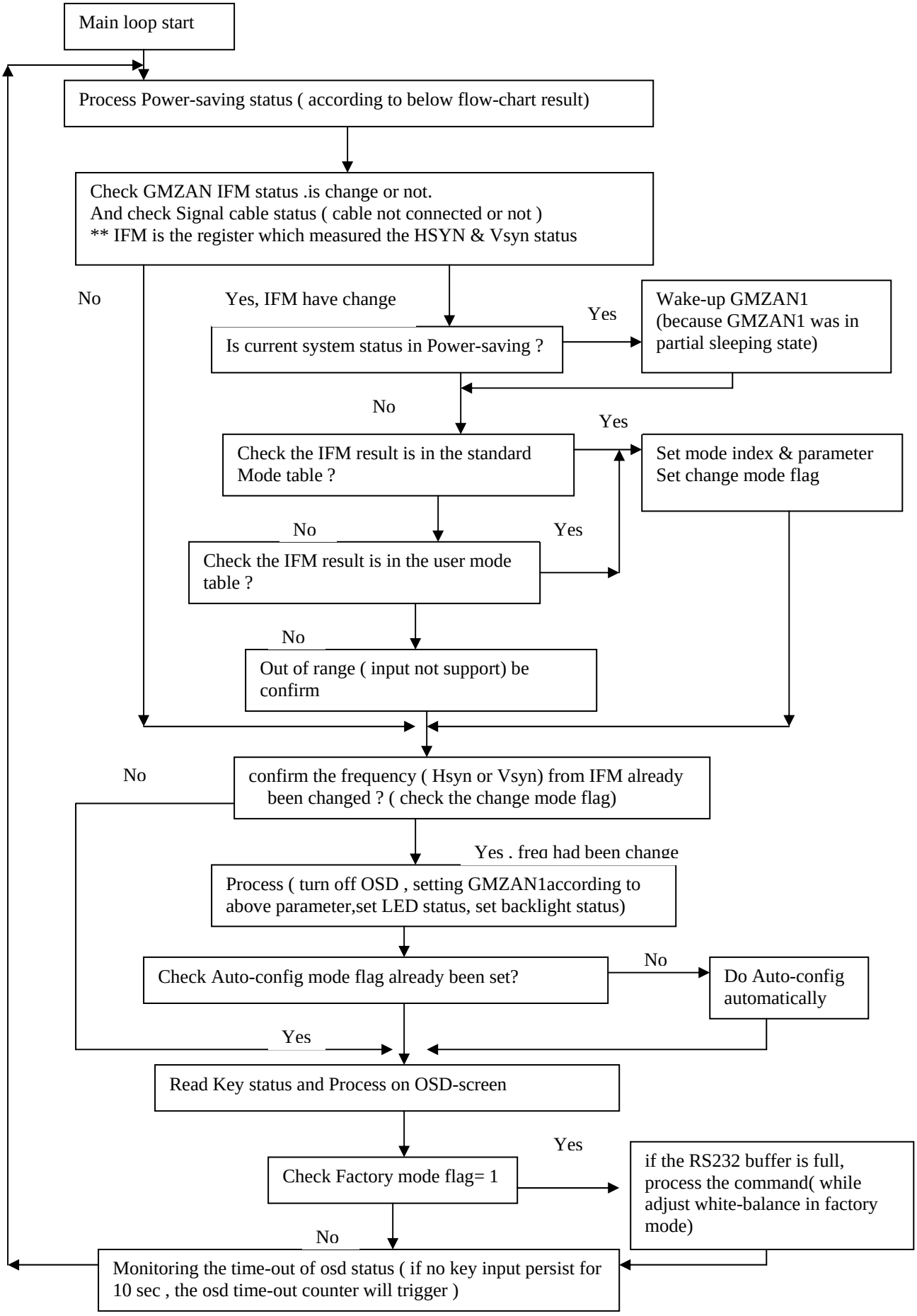


5-4 SOFTWARE FLOW CHART

I. Power-On Subrotine CHART



II. MAIN SUBROTINE LOOP

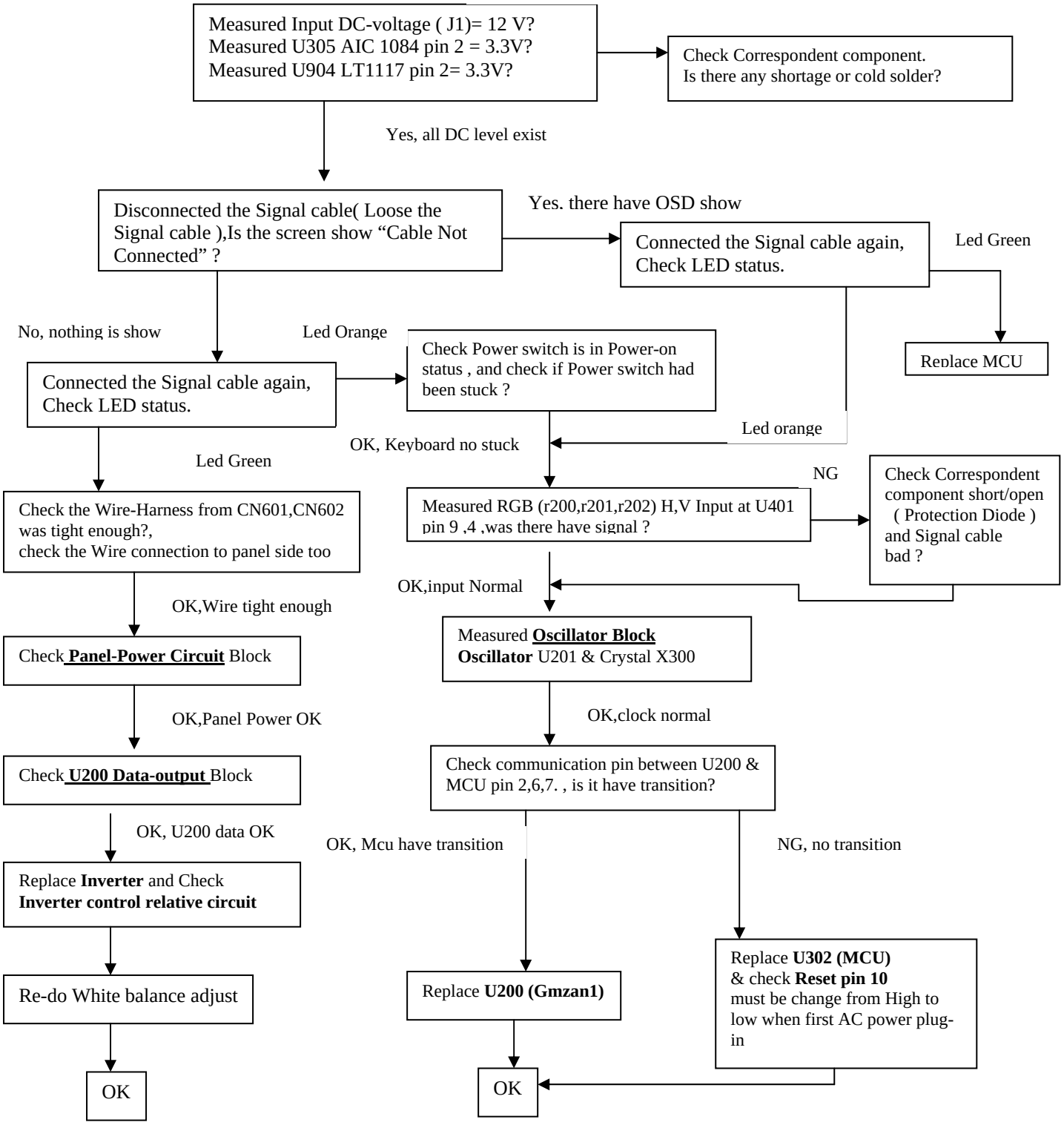


6. A). Interface-Board Trouble-Shooting chart

***Use the PC Win 98 white pattern, with some icon on it, and Change the Resolution to 640x480 60 Hz / 31 KHz**
****NOTICE : The free-running freq. of our system is 48 KHz / 60 Hz, so we recommend to use another resolution to do trouble shooting, this trouble shooting is proceed with 640x480 @60Hz 31Khz**

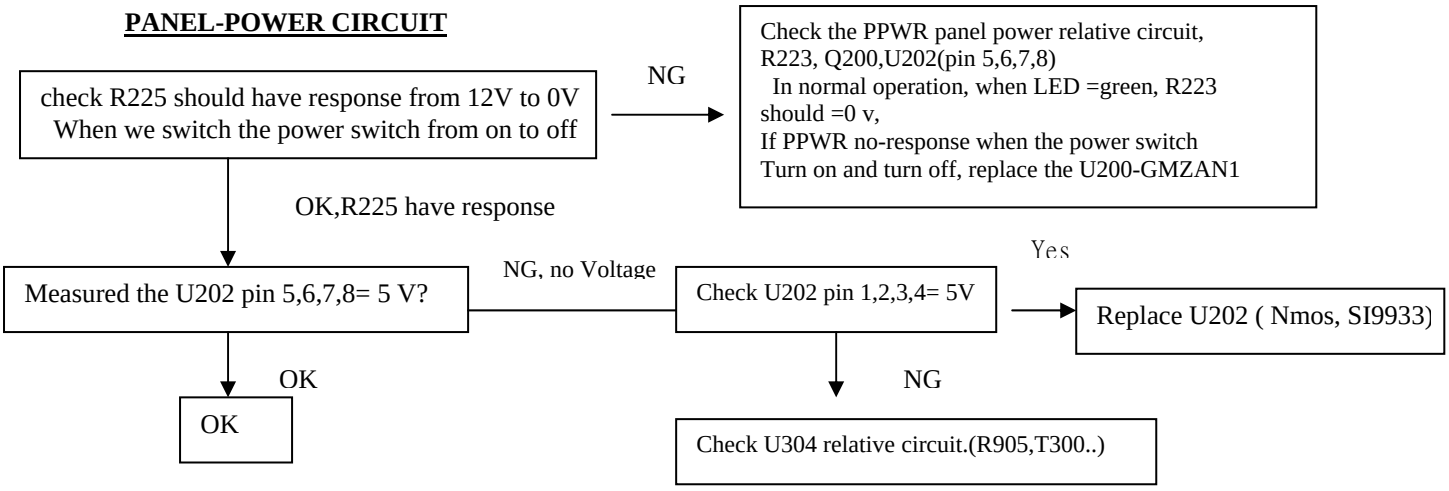
I. NO SCREEN APPEAR

DC-Power Part

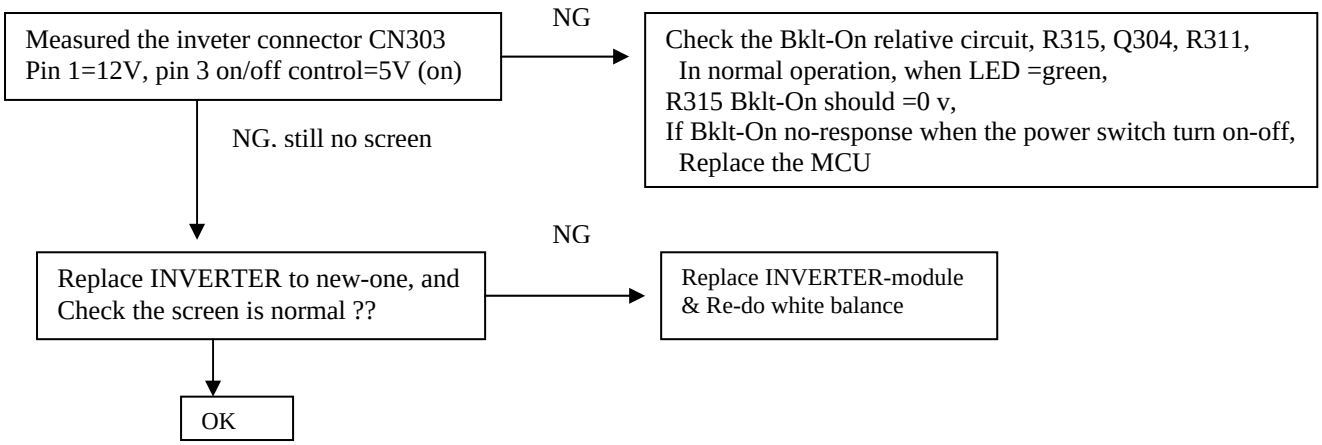


Note: 1. if Replace "**MAIN-BOARD**" , Please re-do "DDC-content" programmed & "WHITE-Balance".
2. if Replace " **INVERTER**" only, Please re-do " WHITE-Balance"

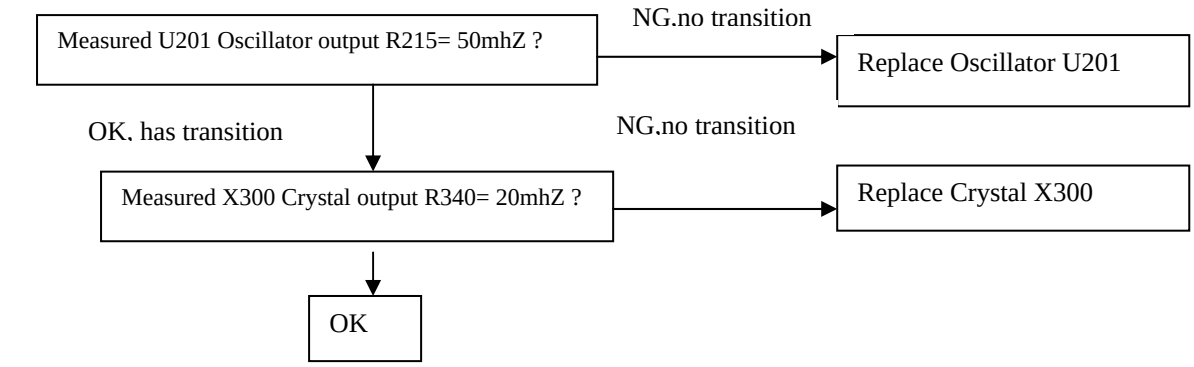
PANEL-POWER CIRCUIT



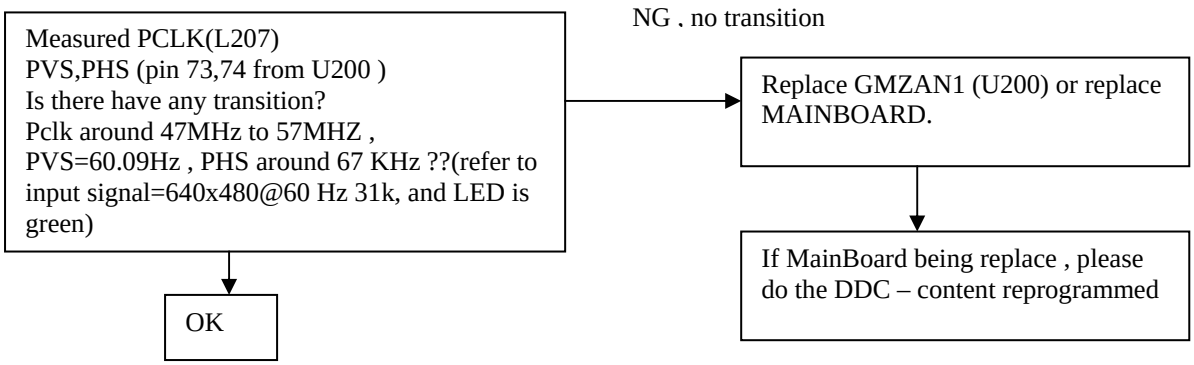
INVERTER Control Relative Circuit



OSCILLATOR BLOCK

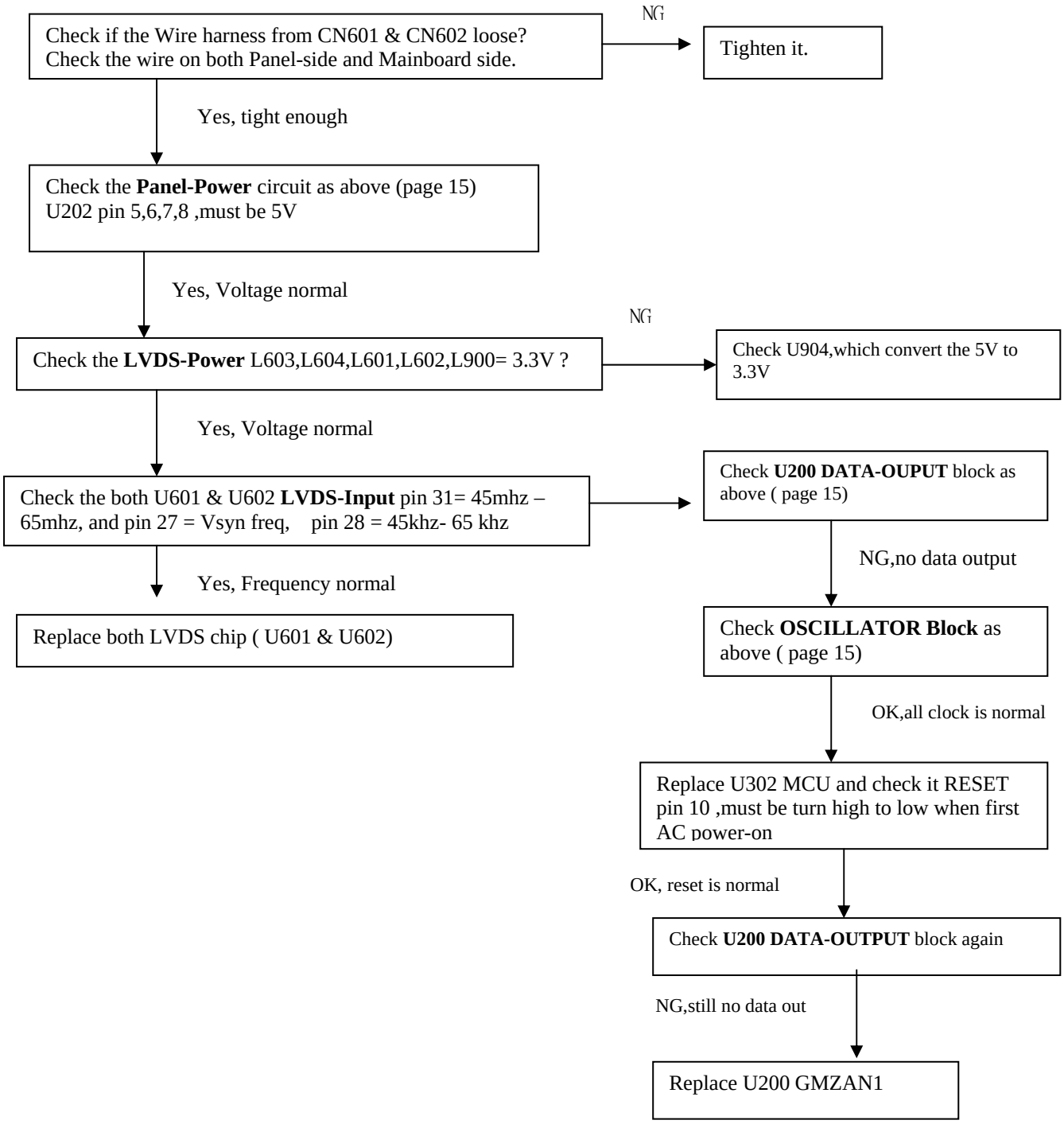


U200-DATA OUTPUT



II (a) THE SCREEN is Abnormal , stuck at white screen, OSD window can't appear, but keyboard & LED was normal operation.

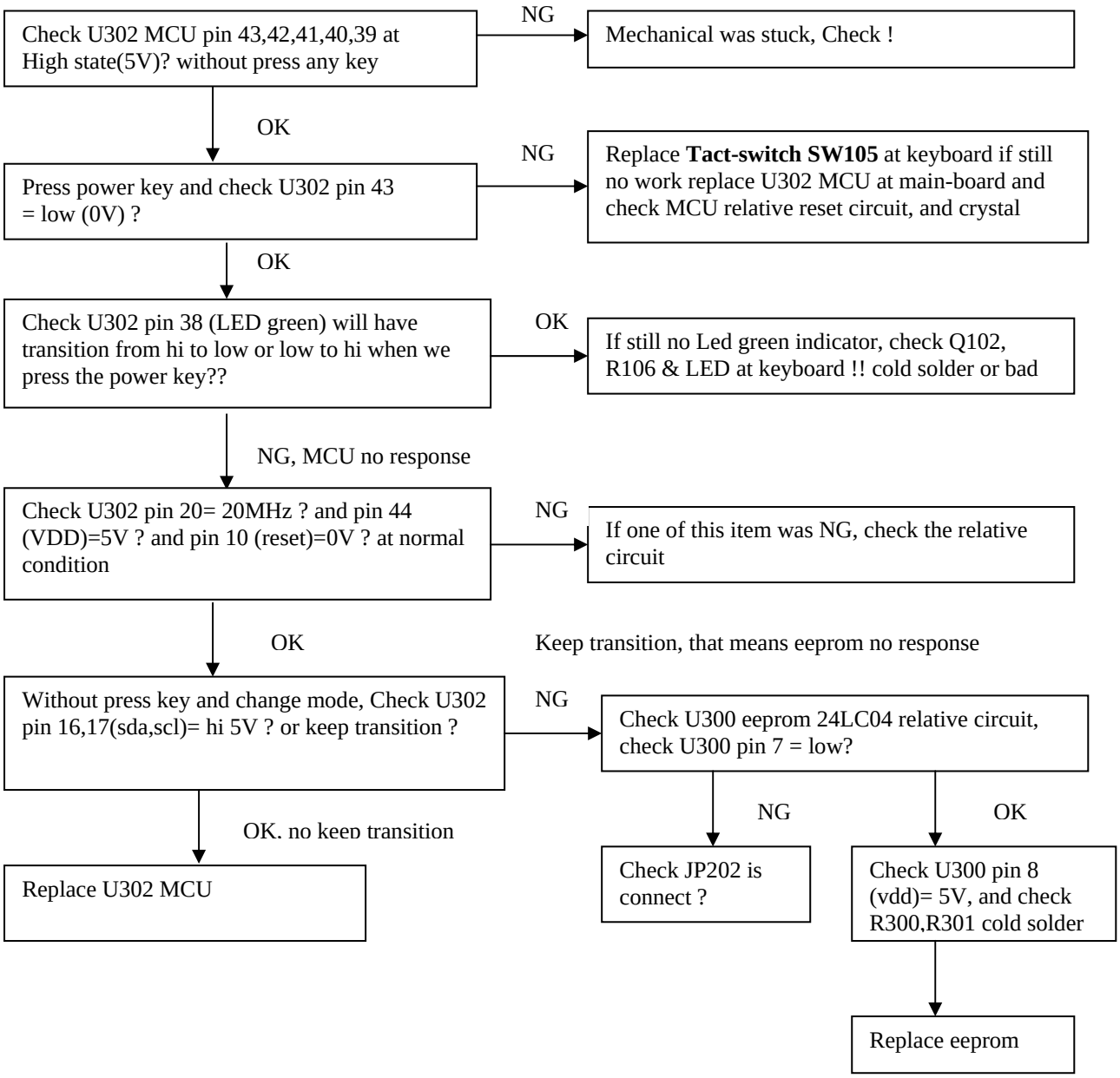
At general, this symtom is cause by missing panel data or panel power, so we must check our wire-harness which connected to panel or the panel power controller (U202)



II. (b)The screen had the Vertical Straight Line, might be stuck in Red, Green, Blue

That symptom is cause by bad Panel issue (might be the Source IC from Panel is cold solder or open loop) so REPLACE THE PANEL TO NEW ONE.

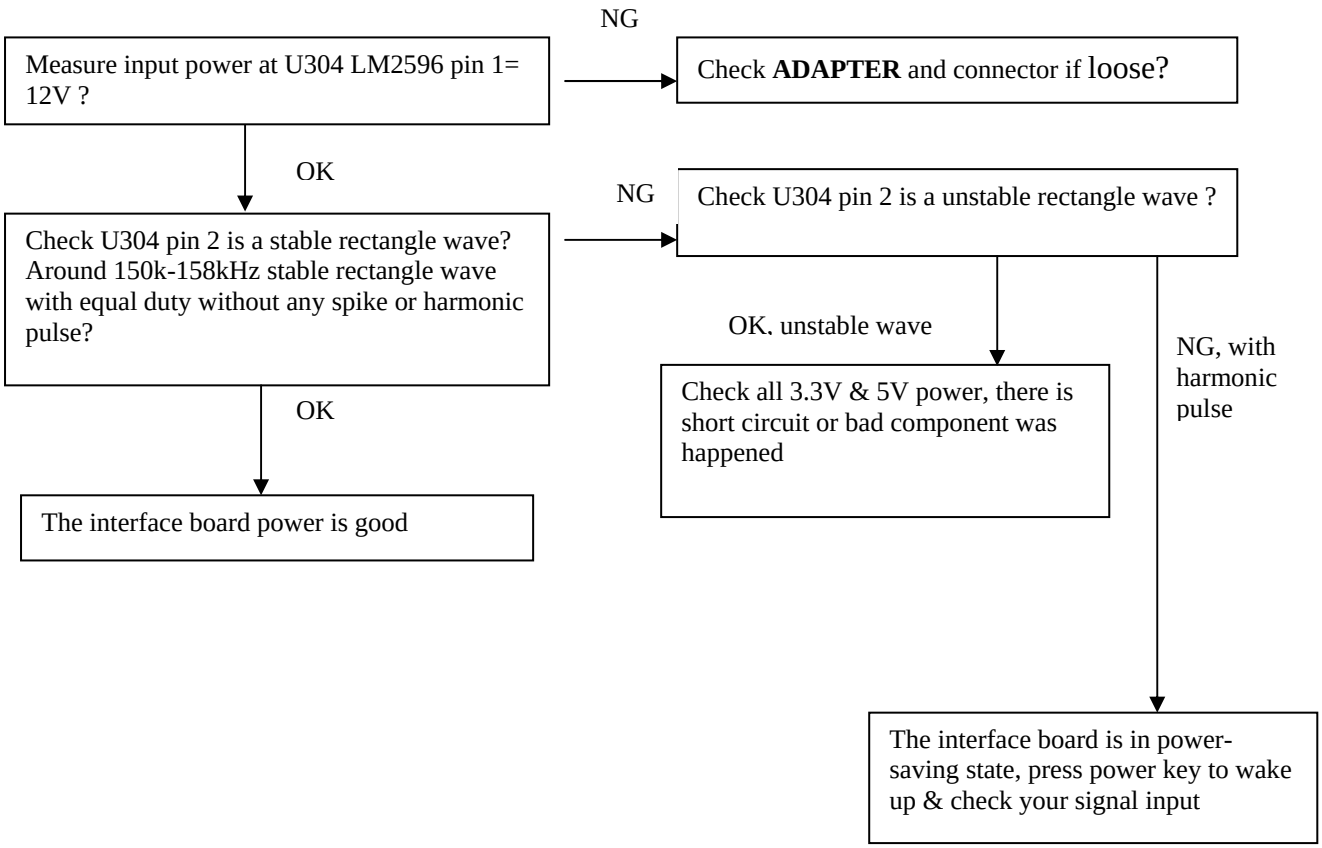
KEYBOARD BLOCK check



POWER-BLOCK check

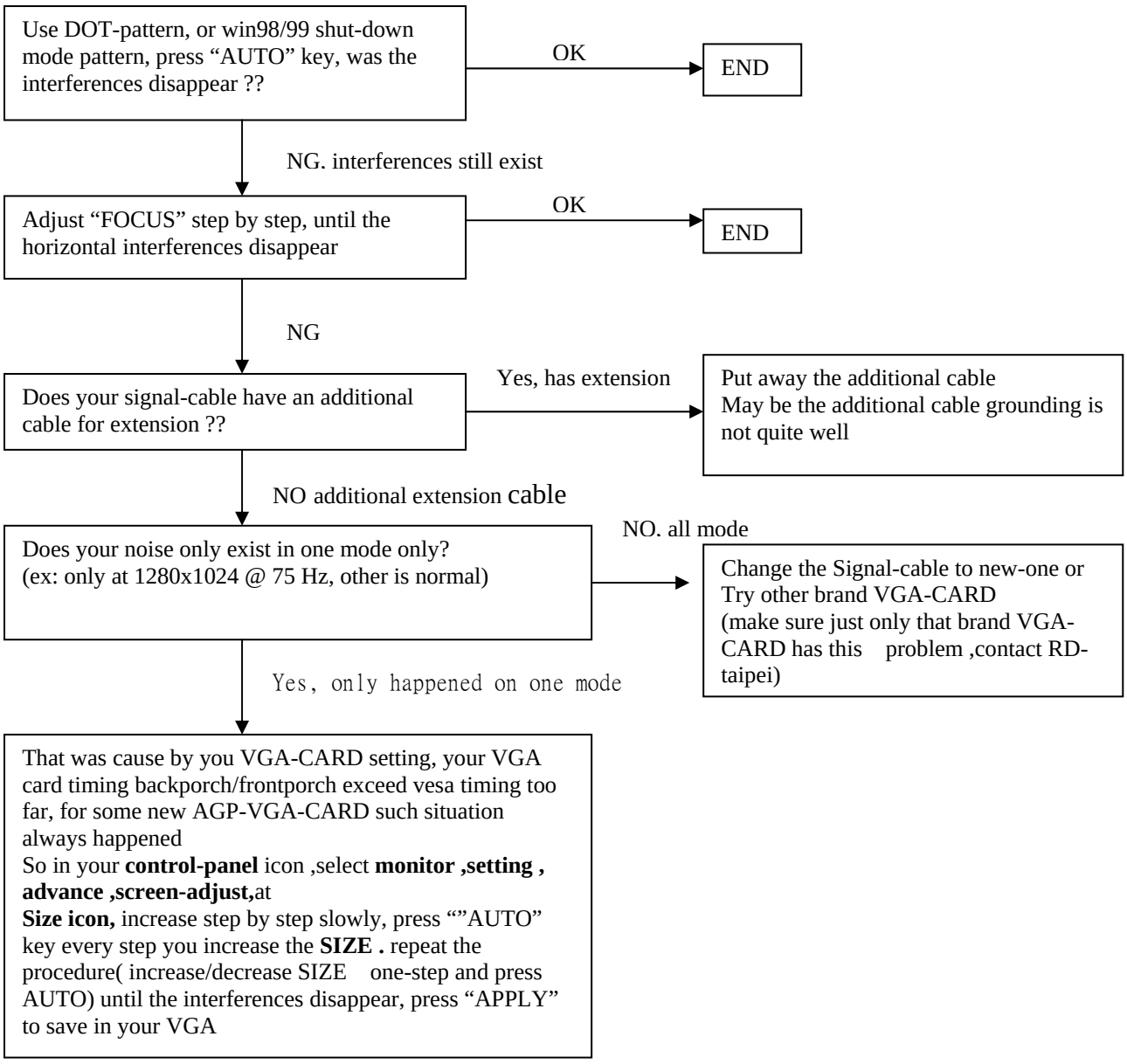
******Note : the Waveform of U304 pin 2 can determined the power situation

1. stable rectangle waveform with equal duty, freq around 150K-158KHz
   that means all power of this interface board is in normal operation
   ,and all status of 5V & 3.3V is working well
2. unstable or uneven rectangle waveform without same duty, that means ABNORMAL operation was happened, check 3.3V or 5V ,if short-circuit or bad component
3. rectangle waveform with large spike & harmonic pulse on front side , means all 3.3v is no load, U200 **Gmzan1** was shut-down, and only U302 **MCU** still working , that means the monitor is in power saving status , all power system is working well .



III.ALL SCREEN HAS INTERFERENCES OR NOISE, CAN'T BE FIXED BY AUTO KEY

**** NOTE:** There is so many kind of interferences, 1). One is cause by some VGA-CARD that not meet VESA spec or power grounding too bad that influence our circuit
2).other is cause by external interferences, move the monitor far from electronic equipment.(rarely happened)



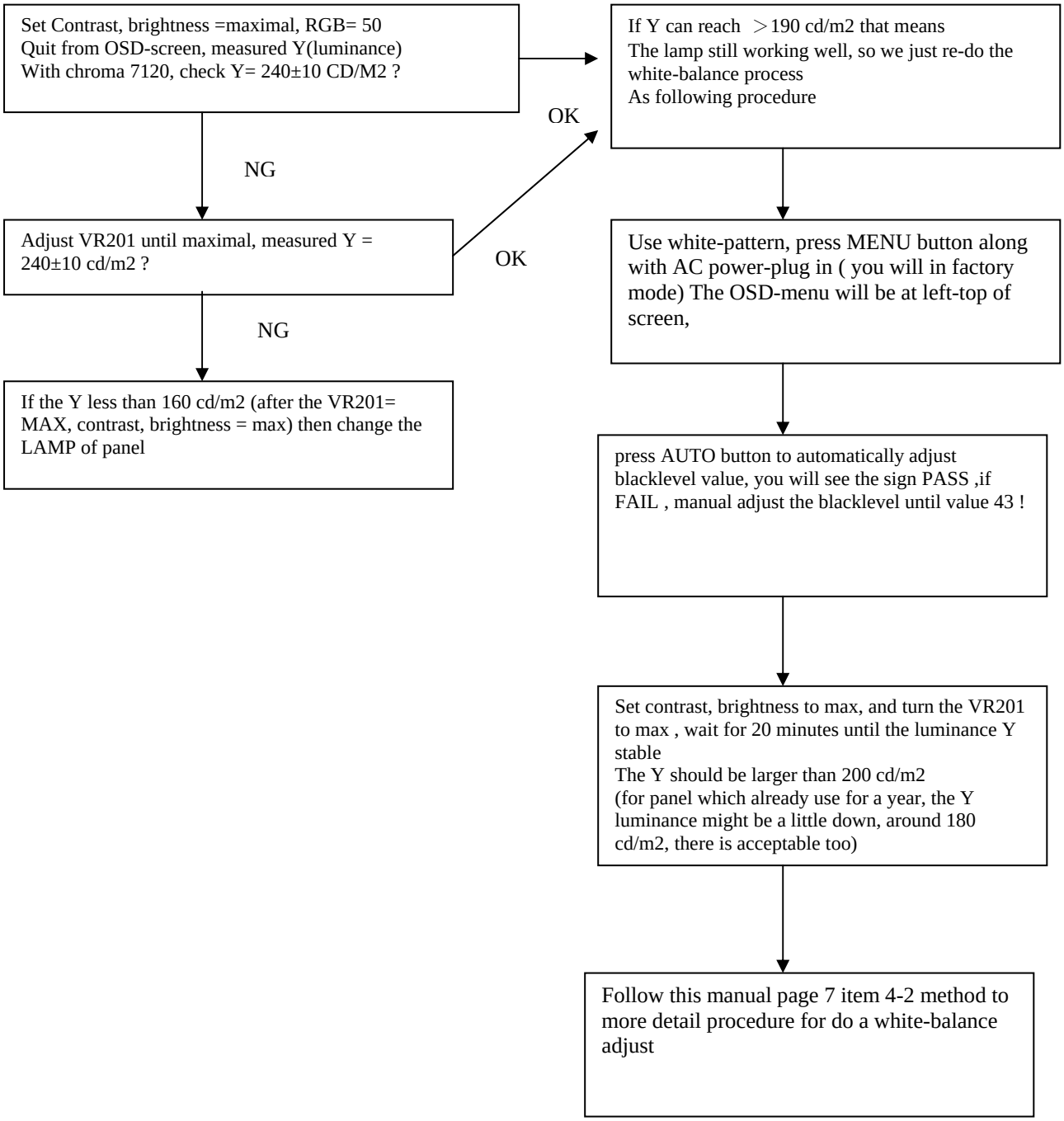
There is an interferences in **DOS MODE**

NOTE :the criteria of doing AUTO-CONFIGURATION : must be a full-size screen, if the screen not full , the auto-configuration will fail. So in dos mode ,just set your "CLOCK" in OSD-MENU to zero or use some EDITOR software which can full fill the whole screen (ex: PE2, HE) and then press "AUTO"

Or you can use "DOS1.EXE" which attached in your Driver disk to optimize DOS mode performance

V.THE PANEL LUMINANCE WAS DOWN

Use white pattern and resolution 1280x1024 @ 60Hz , CHROMA 7120 measured the center of panel



6 B). Inverter –MODULE Spec &Trouble Shooting Chart

In LM700 model , we use CHI-MEI panel, and the INVERTER PROVIDER is SAMPO-CORPORATION

I.) TROUBLE SHOOTING OF CHI-MEI INVERTER (part no : 79AL17-1-S)

TYPE: L0037 FOR CHI-MEI 17”PANEL

SAMPO CORPORATION

TROUBLE SHOOTING OF CHI-MEI INVERTER (DIVTL0037-D42- -)

1.SAMPO PART NO .: L0037 ,AOC PART NO.: 79AL17-1-S

2.SCOPE : this is to specify the requirements of the subject parts used in CHI-MEI (M170E1) 17 inch (4 C.C.F.L.) LCD monitor.

3.CONNECTOR PIN ASSIGMENT:

4-1. CON1: INPUT

MODEL NO.: S5B-PH-SM3-TB

PIN	SYMBOL	DESCRIPTION
1	Vin	Input voltage: 12V
2	Vin	Input voltage: 12V
3	ON/OFF	ON: 3V OFF:0V
4	Dimming	Dimming range (0V~+5.0V)
5	GND	GND

4-2. CON2,CON3 : OUTPUT

MODEL NO. : SM04(4.0)B-BHS-1-TB

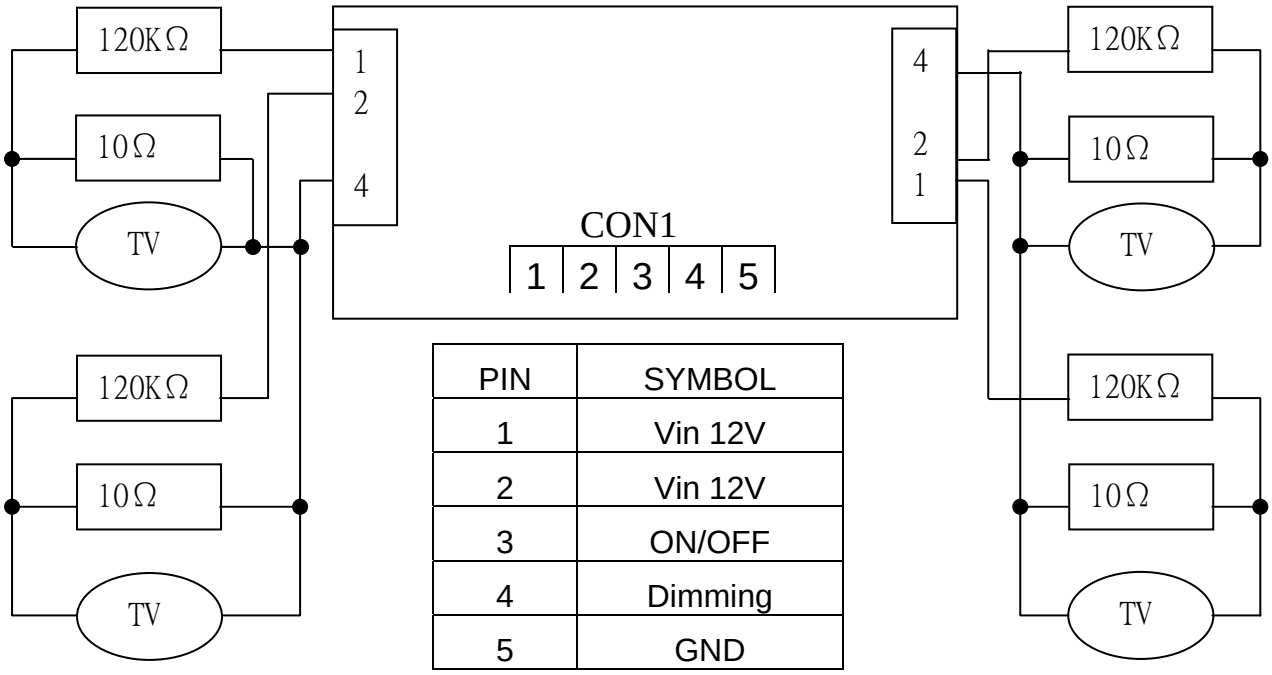
PIN	SYMBOL	DESCRIPTION
1	HV OUTPUT	Input H.V to lamps
2	HV OUTPUT	Input H.V to lamps
3	N.C.	N.C.
4	RETURN	Return to control

5.FUNCTION SPECIFICATIONS:

The data test with the set of SAMPO, and the test circuit is as below.

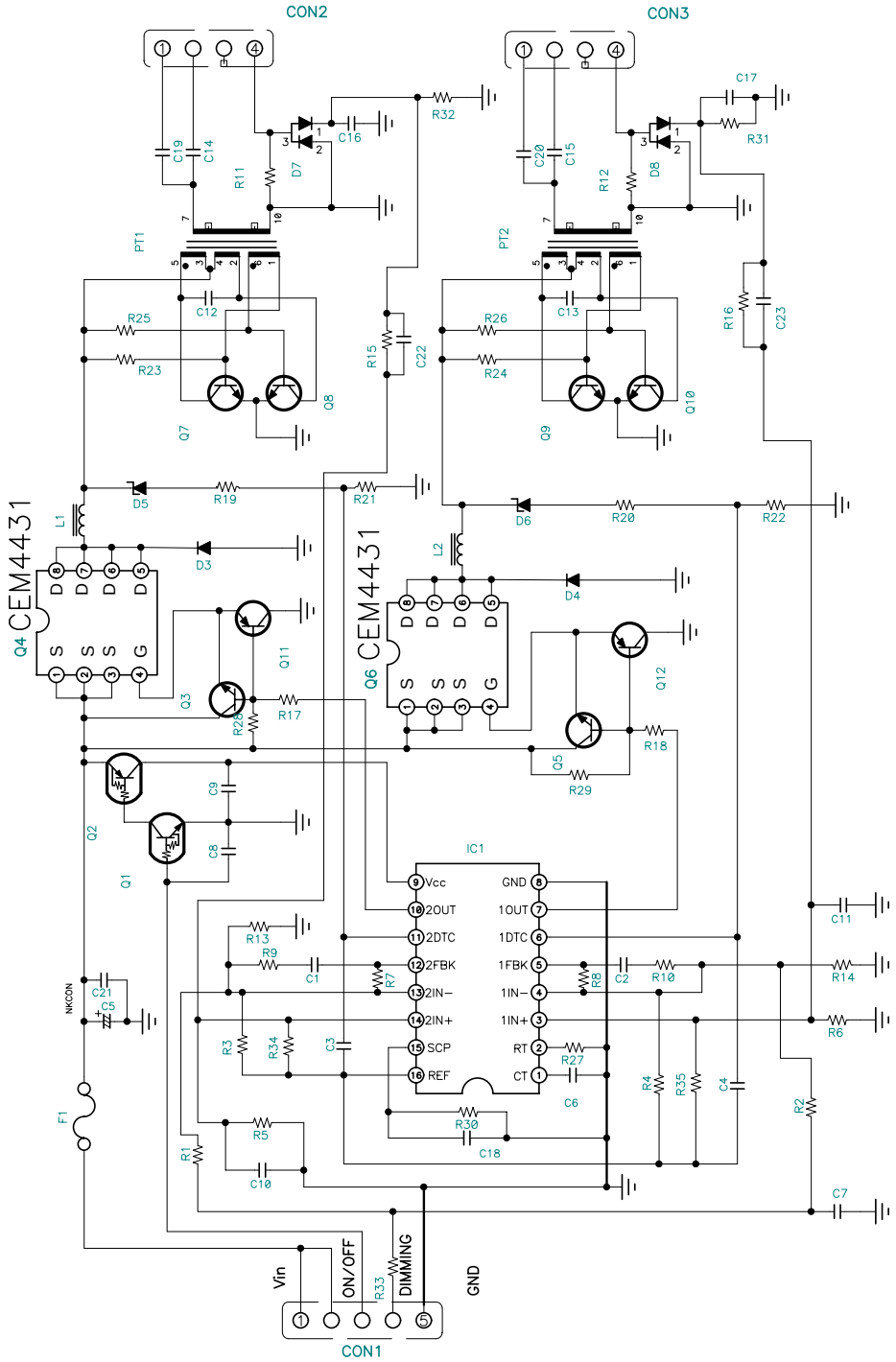
ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARK
Input voltage	Vin	10.8	12	13.2	V	
Input current	Iin	--	2200	2500	mA	
output current adj:0v(min.)	Iout (min)	2.1	2.6	3.1	mA	FOR 1 CCFL LOAD:120KΩ
Output current adj.:5 v(max.)	Iout (max)	5.5	6.0	6.5	mA	FOR 1 CCFL LOAD:120KΩ
Frequency	F	40	50	60	KHZ	
H.V open	Vopen	1400	1500	1600	Vrms	NO LOAD
H.V Load	Vload	630	730	830	Vrms	RL=120KΩ

6. FUNCTION LOAD CIRCUIT:



PIN	SYMBOL
1	Vin 12V
2	Vin 12V
3	ON/OFF
4	Dimming
5	GND

7.CIRCUIT DIAGRAM:



8.PART LIST

8-1 COMPONENTS LIST:

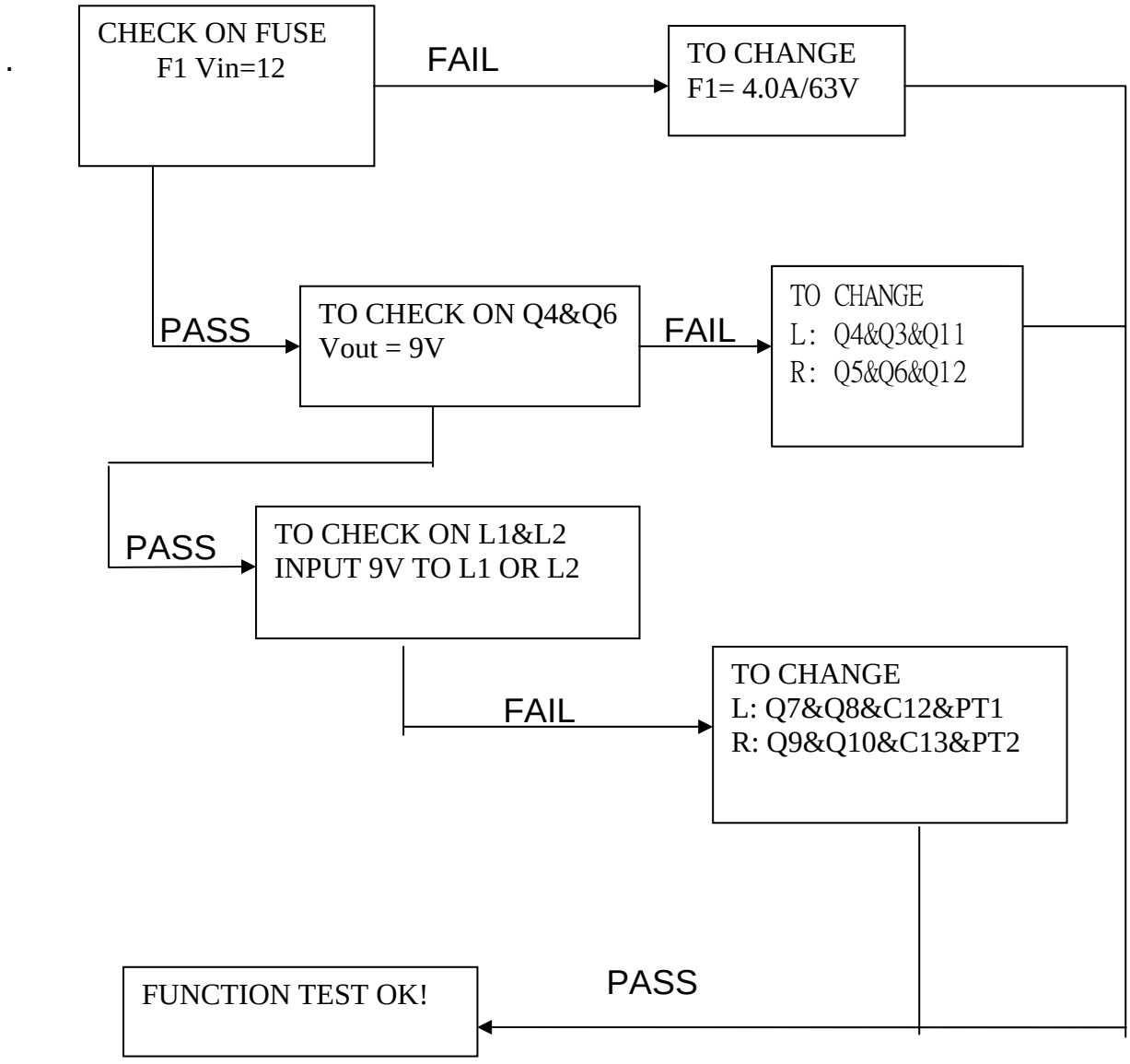
NO.	REF.	PART NAME	PART NUMBER	QTY	DESCRIPTION	SUPPLIER	REMARK
1.	CON1	CONNECTOR	VCNCP0015-EJSTA	1	S5B-PH-SM3-TB	JST	
2.	CON2,3	〃	VCNCP0014-PJSTA VCNCP0014-ZGLEA	2	SM04(4.0)B.BHS-1-TB GL SM02(4.0)-WH2	JST GEAN-LEA	
3.	R1,2	RESISTOR	VRMHNVA--103J-A	2	SMD 0603 10KΩ 5%	YAGEO	
4.	R3,4	〃	VRMHNVA--683J-A	2	SMD 0603 68KΩ 5%	YAGEO	
5.	R5,6	〃	VRMHNVA--912J-A	2	SMD 0603 9.1KΩ 5%	YAGEO	
6.	R7,8	〃	VRMHNVA--274J-A	2	SMD 0603 270KΩ 5%	YAGEO	
7.	R9,10	〃	VRMHNVA--R00J-A	2	SMD 0603 0Ω 5%	YAGEO	
8.	R11,12, 31,32	〃	VRMCNV8--102F-A	4	SMD 0805 1KΩ 1%	YAGEO	
9.	R13,14	〃	VRMHNVA--752J-A	2	SMD 0603 7.5KΩ 5%	YAGEO	
10.	R15,16	〃	VRMHNVA--433J-A	2	SMD 0603 43KΩ 5%	YAGEO	
11.	R17,18	〃	VRMHNVA--271J-A	2	SMD 0603 270Ω 5%	YAGEO	
12.	R27	〃	VRMHNVA--472J-A	1	SMD 0603 4.7KΩ 5%	YAGEO	
13.	R28,29,	〃	VRMHNVA--392J-A	2	SMD 0603 3.9KΩ 5%	YAGEO	
14.	R23,24, 25,26	〃	VRMBNV4--102F-A	4	SMD 1206 1KΩ 1%	YAGEO	
15.	R19,20	〃	VRMCNV8--183F-A	2	SMD 0805 18KΩ 1%	YAGEO	
16.	R21,22	〃	VRMCNV8--133F-A	2	SMD 0805 13KΩ 1%	YAGEO	
17.	R33	〃	VRMHNVA--363J-A	1	SMD 0603 36KΩ 5%	YAGEO	
18.	Q1	TRANSIST0R	VSTDTC144WKA--A	1	SMD DTC144WKA	ROHM	
19.	Q2	〃	VSTDTA144WKA--A	1	SMD DTA144WKA	ROHM	
20.	Q3,5	〃	VSTSST3904----A VSTMMBT3904-A	2	SMD SST3904-T116 SMD MMBT3904	ROHM MOTOROLA	
21.	Q4,6	〃	VSTCEM9435A-----A	2	SMD CEM9435A	CET	
22.	Q7,8,9, 10	〃	VST2SD2150----A	4	SMD 2SD2150	ROHM	
23.	C1,2	CAPACITOR	VCLFCN1EY224Z-A	2	SMD 0805 0.22 μF/25V	TDK	
24.	C3,4,,9	〃	VCLRCN1EB104K-A	3	SMD 0805 0.1 μF/25V	TDK	
25.	C5		VCEATU1EC336M-- VCEATU1VC476M--	1	DIP UGX 33 μF/25V DIP UGX 47 μF/35V	SANYO	

8-2 COMPONENTS LIST:

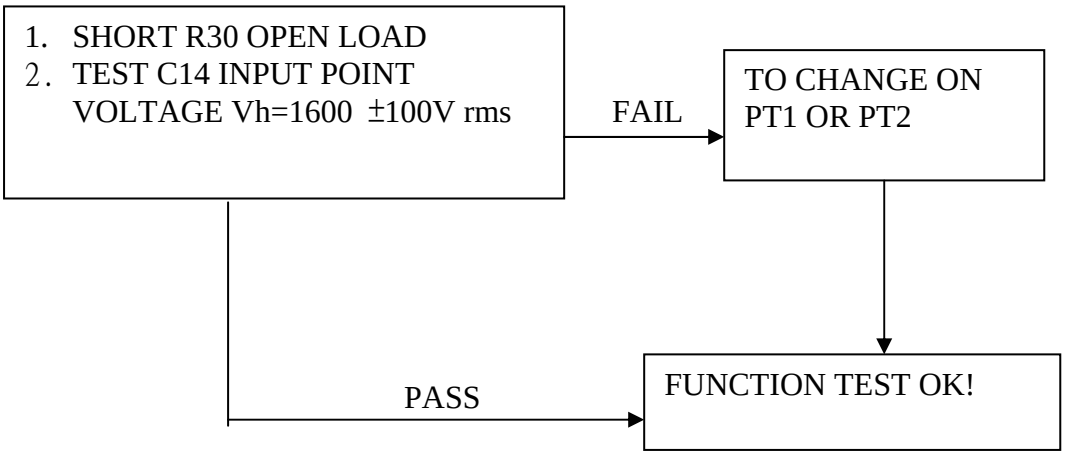
NO.	REF.	PART NAME	PART NUMBER	QTY	DESCRIPTION	SUPPLIER	REMARK
26.	C6	〃	VCLRCN1HB102K-A	1	SMD 0805 1000PF/50V	TDK	
27.	C10,11	〃	VCLRCN1EB333K-A	2	SMD 0805 0.033 μF/25V	TDK	
28.	C12,13	〃	VCMEBF2AB184J-P VCMECF2AC184J-P	2	DIP 0.18μF/100V DIP 0.18μF/100V	ARCO THOMSON	
29	C14,15,19, 20	CAPACITOR	VCDSEU3SL220K--	4	DIP 22PF/3KV 10%	TDK	
30.	C7,16,17	〃	VCLFCN1EY105Z-A	3	SMD 0805 1 μF/25V	TDK	
31.	C18	〃	VCLFCN1CY225Z-A	1	SMD 0805 2.2 μF/16V	TDK	
32.	C21	〃	VCLFBN1CY475Z-A	1	SMD 0805 4.7 μF/16V	TDK	
33.	D1,2	DIODE	VSDRLS4148----A	2	SMD RLS4148	ROHM	
34.	D3,4	〃	VSDRB160L40---A VSDSMA160-----A	2	SMD RB160L40 SMD SMA160	ROHM TPC	
35.	D5,6	〃	VSZRLZ8.2B-----A	2	SMD RLZ8.2B	ROHM	
36.	D7,8	〃	VSDDA204K-----A	2	SMD DA204K	ROHM	
37.	I.C	I.C	VSITL1451ACNS-A	1	SMD TL1451ACNS	TEXAS	
38.	F1	FUSE	QFS-N302FIDZD-A QFS-Z302FIDZD-A	1	SMD FUSE 3.0A/63 SMD FUSE 3.0A/63	LITTLE BUSSMANN	Attachment (FEC1Q2)
40.	L1,2	COIL	RCHOL0007ID151A RCHOL0007ID151-	2	DIP 150μH 10% DIP 150μH 10%	YST 弦 赫	Attachment 1
41.	PT1,2	TRANS	RCVT-1207ID-Z-A RCVT-1207ID-Z-C	2	SMD YST-1207 SMD WT-1207	YST WT	Attachment 2 Attachment 2-1
42.	PCB	PCB	QPWBGL983IDLF3-	1	QPWBGL983IDLF3-	EISO LONGMAW 千友	

9. TROUBLE SHOOTING

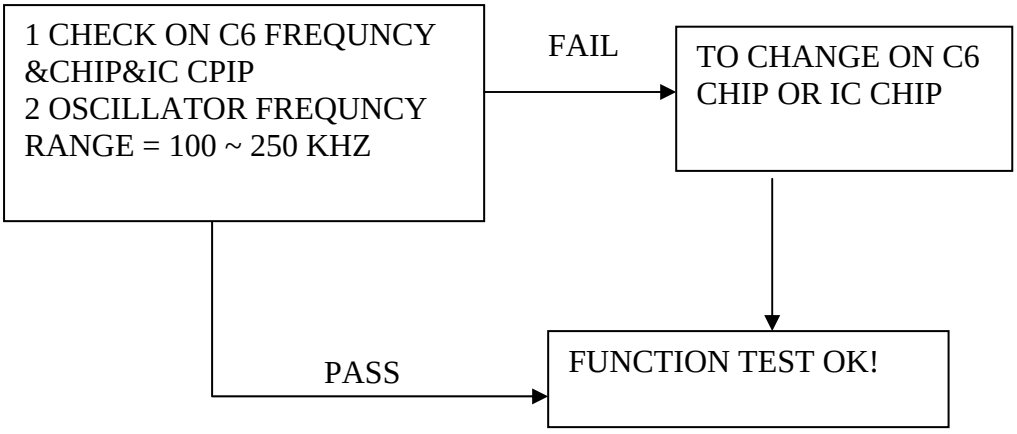
9-1 NO POWER:



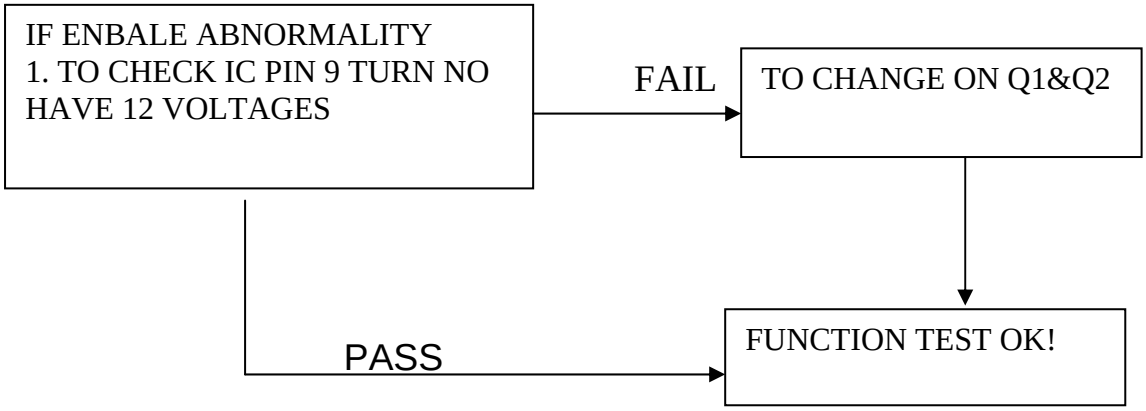
9-2 HIGHT VOLTAGE PROTECTION:



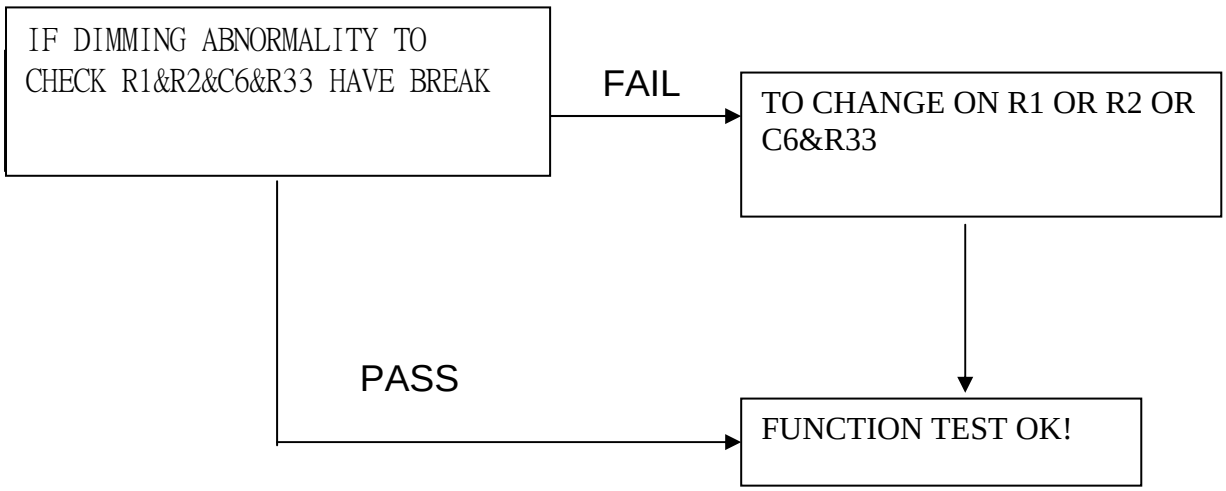
9-3 OUTPUT CURRENT ABNORMALITY:



9-4. ENBALE ABNORMALITY:



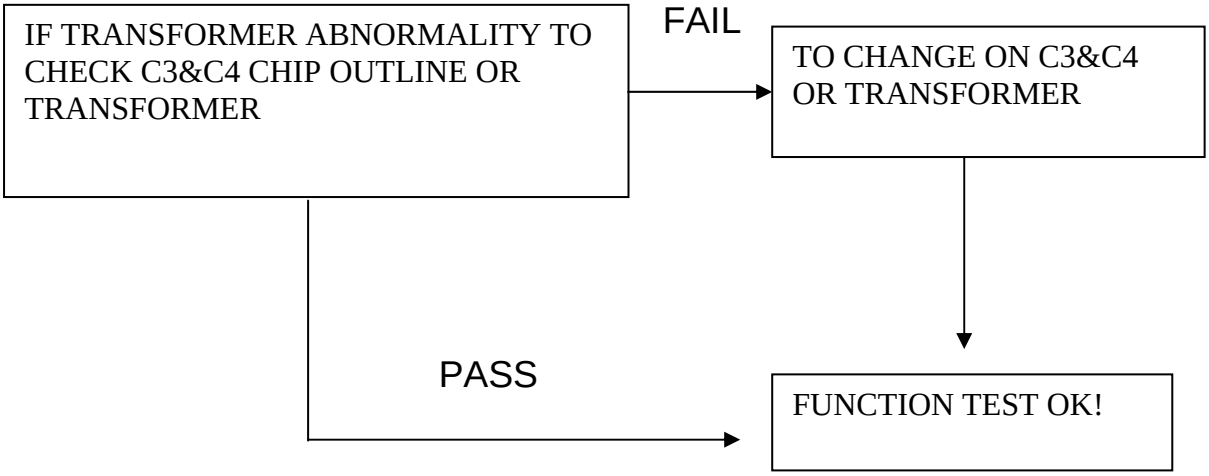
9-5 DIMMING CONTROL ABNORMALITY:



SAMPO CORPORATION

TROUBLE SHOOTING OF CHI-MEI INVERTER (DIVTL0037-D42- -)

9-6 TRANSFORMER ABNORMALITY:



10. INSTRUMENTS FOR TEST:

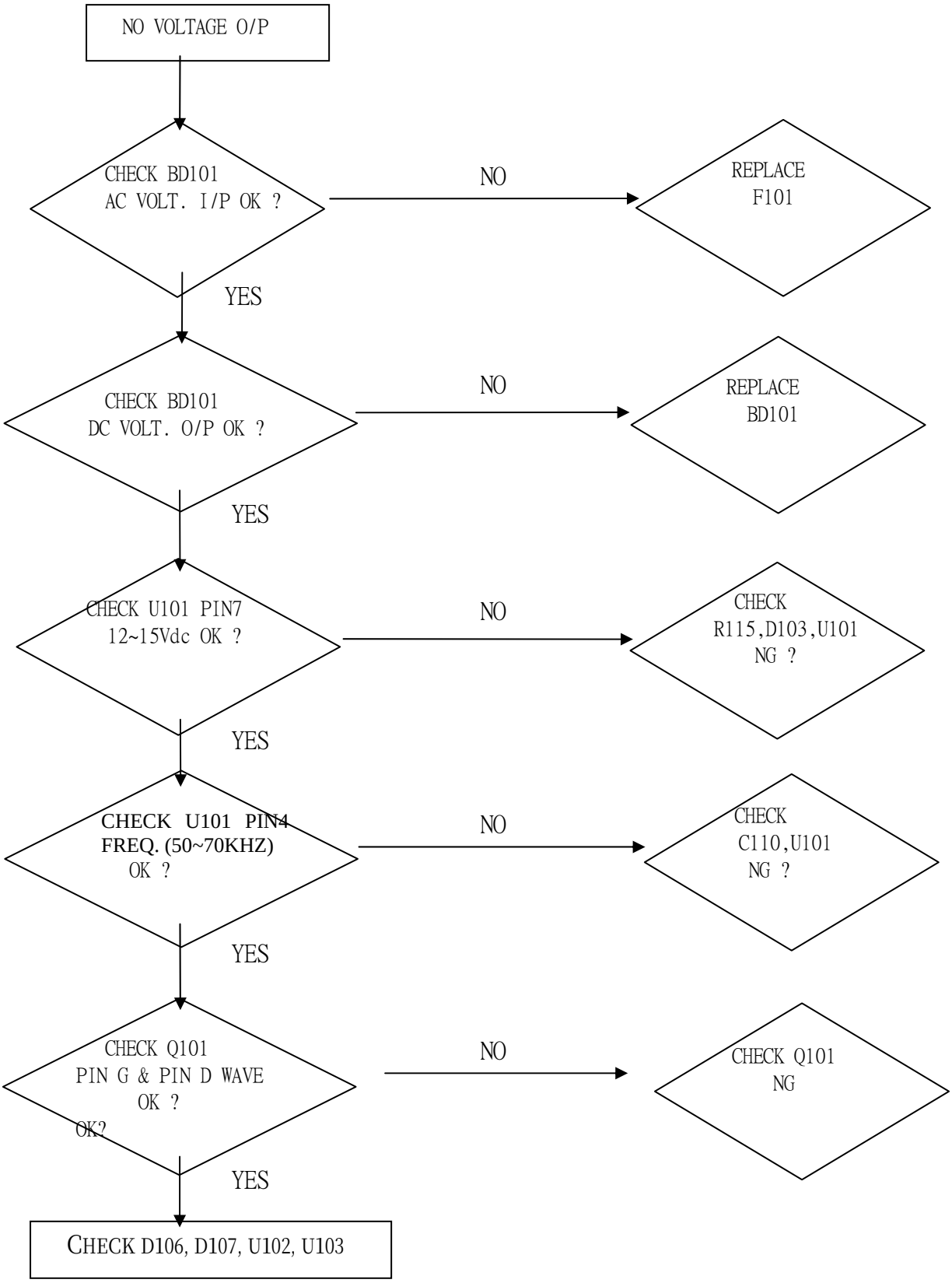
1. DC POWER SUPPLY	GPS-3030D
2. AC VTVM	VT:-181E
3. DIGITAL MULTIMERTER	MODEL-34401
4. HIGHTVOLT PROB	MODEL-1137A
5.SCOPE	MODEL-V-6545
6. AC mA METER	MODEL-2016 (YOKOGAWA)

6 C). ADAPTER-MODULE Trouble shooting chart

The following spec & block-diagram is offer by CHI-SAM –COMPANY, for External Adapter

part number : 80AL17-1-CH (Black), 80AL17-2-CH (White)

AC ADAPTER CH-1205 TROUBLE SHOOTING



I.) Adapter Schematic CH-1205

Please see the ADAPTER-SCHEMATIC in the end of this Document (page 75)

IV. ADAPTER BOM LIST (PART no. 80AL15-2-LI)

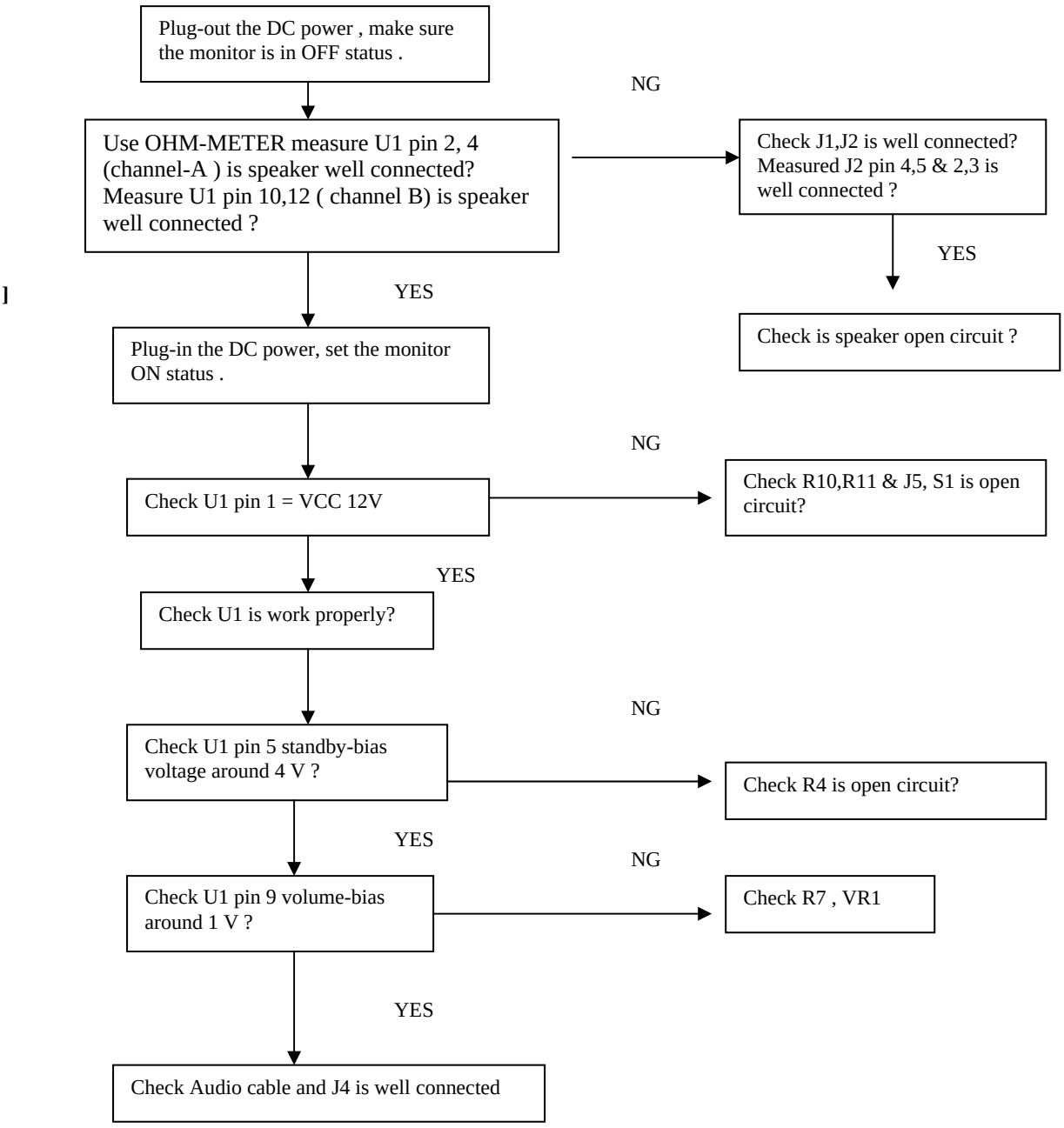
Item	Reference	Part	Quantity	Cat.NO.
1	BD101	DIODE BRIDGE KBL405G 600V/4A	1 PCS	15D7L405G6
2	CN101	AC POWER SOCKET	1 PCS	64P21-0001
3	BEAD1,BEAD2,BEAD3,BEAD4	BEAD 3.5*3.2*1.6mm	4 PCS	62C-353216
4	C116	CAP CER 102P/500V +-10% Y5P	1 PCS	99426A1025
5	C105	CAP CER 103P/500V +80-20% Z5V	1 PCS	99459F1033
6	C107,C108,C109, C121,C122,C123	CAP CER 104P/50V +-10% X7R SMD(0805)	6 PCS	99B26D104D
7	C112	CAP CER 271P/50V +-5% NPO SMD(0805)	1 PCS	99B15E271D
8	C113	CAP CER 301P/50V +-5% NPO SMD(0805)	1 PCS	99B15E301D
9	C110,C111	CAP CER 332P/50V +-10% X7R SMD(1206)	2 PCS	99B26D332E
10	C114	CAP CER 102P/50V +-10% X7R SMD(0805)	1 PCS	99B26D102D
11	C117,C118	CAP ELEC 1000U/16V +-20% 105℃(LOW ESR)	2 PCS	28D37-1021
12	C104	CAP ELEC 120U/400V +-20% 105℃ 650mA 18*36	1 PCS	281D701211
13	C106	CAP ELEC 150U/25V +-20% 105℃	1 PCS	28147-1511
14	C119	CAP ELEC 470U/16V +-20% 105℃(LOW ESR)	1 PCS	28D37-4711
15	C103	CAP X1 0.47U/300Vac +-10% P=22.5	1 PCS	42A96-474G
16	C124	CAP Y2 102P/250Vac +-20% P=7.5，長腳	1 PCS	42D77-102F
17	C101,C102,C115	CAP Y2 222P/250Vac +-20% P=7.5	3 PCS	42D77-222F
18	L103	COIL CHOKE 5uH 5*20(RD005)	1 PCS	45M56-509C
19	D104,D105,D108,D109	DIODE 1N4148 75V/150mA(SMD)	4 PCS	15A2N41480
20	D102,D103	DIODE RLS245(SMD)	2 PCS	15AHLS2450
21	D106,D107	DIODE SCHOTTKY MBR20100CT 100V/20A	2 PCS	15B3100CT6
		DIODE SCHOTTKY MBRF20100CT 100V/20A		15B3201006
		DIODE SCHOTTKY FCH20A10 100V/20A		15B320A106
		DIODE SCHOTTKY SS20FJK10L 100V/20A		15B3JK10L6
22	D101	DIODE UF4005G 600V/1A	1 PCS	15A74005G2
23	ZD102	DIODE ZENER RLZ18C(SMD)	1 PCS	15Z35Z18C0
24	ZD101	DIODE ZENER RLZ20B(SMD)	1 PCS	15Z35Z20B0
25	FOR COVER SCREW	PHM3-20*10	2 pcs	6721A30101
26	F101	FUSE T2A/250Vac SLOW BLOW	1 PCS	49F54-202A
27	U105	IC AP431W*D 85℃ SMD(SOT-23)	1 PCS	171AP431WD
28	U104A	IC BA10358F(SMD)	1 PCS	171A10358F
29	U101	IC CM3842	1 PCS	1700CM3842
30	U103	IC CM431	1 PCS	17000CM431
31	U102	IC H11A817C	1 PCS	17011A817C
32	J101	JUMPER 0.6φ 8*12.5mm	1 PCS	54JB5-0005
34	J104	JUMPER 0.6φ 8*22.5mm	1 PCS	54JB5-0009
35	J103,J105,J106	JUMPER 0.6φ 8*5mm	3 PCS	54JB5-0002
36	J102	JUMPER 0.6φ 8*7.5mm	1 PCS	54JB5-0003
37	LED101	LED L-34GD TYPE GREEN	1 PCS	1903112011
38	L102	LINE FILTER 18mH UU15.7(RD002)	1 PCS	47E10-0010
39	Q101	MOS FET 2SK2996 600V/10A	1 PCS	14K1SK2996
		MOS FET2SK2761-01MR 600V//10A		14K1SK2761
		MOS FET 2SK2843 600V/10A		14K1SK2843
40	R101	NTCR 3 OHM/5A 10φ +-15%	1 PCS	26B2L50011

41	PCB	PCB FOR CH-1205 REV:D	1 PCS	11S43-0030
42	R117	RES 100 1/8W +-5% SMD(0805)	1 PCS	2242510000
43	J109,J110	RES 0 OHM 1/4W +-5% SMD(1206)	2 PCS	2243500000
44	R143	RES 1.8K 1/8W +-5% SMD(0805)	1 PCS	2242518010
45	R114	RES 100 1/4W +-5% SMD(1206)	1 PCS	2243510000
46	R124,R127	RES 10K 1/8W +-5% SMD(0805)	2 PCS	2242510020
47	R136	RES 113K 1/8W +-1% SMD(0805)	1 PCS	2242111330
48	R145	RES 12K 1/4W +-5% SMD(1206)	1 PCS	2243512020
49	R128	RES 13K 1/8W +-5% SMD(0805)	1 PCS	2242513020
50	R115	RES 15 1/4W +-5% SMD(1206)	1 PCS	2243515090
51	R123	RES 150 1/4W +-5% SMD(1206)	1 PCS	2243515000
52	R107,R108,R109,R110	RES 180K 1/4W +-5% SMD(1206)	4 PCS	2243518030
53	R142	RES 2.4K 1/8W +-1% SMD(0805)	1 PCS	2242124010
54	R130,R131,R132, R133	RES 24 1/4W +-5% SMD(1206)	4 PCS	2243524090
55	R141	RES 270 1/4W +-5% SMD(1206)	1 PCS	2243527000
56	R129	RES 3.6K 1/8W +-5% SMD(0805)	1 PCS	2242536010
57	R137	RES 3.74K 1/8W +-1% SMD(0805)	1 PCS	2242137410
58	R139	RES 330 1/4W +-5% SMD(1206)	1 PCS	2243533000
59	R105,R106	RES 3M 1/4W +-5% SMD(1206)	2 PCS	2243530040
60	R104,R116	RES 4.7K 1/4W +-5% SMD(1206)	2 PCS	2243547010
61	R118,R144,R120,R134	RES 4.7K 1/8W +-5% SMD(0805)	4 PCS	2242547010
62	R102,R103	RES 470K 1/4W +-5% SMD(1206)	2 PCS	2243547030
63	R122	RES 47K 1/8W +-5% SMD(0805)	1 PCS	2242547020
64	R126	RES 510 1/8W +-5% SMD(0805)	1 PCS	2242551000
65	R138	RES 680 1/8W +-1% SMD(0805)	1 PCS	2242168000
66	R121	RES 8.2K 1/8W +-1% SMD(0805)	1 PCS	2242182010
67	R140	RES 9.31K 1/8W +-1% SMD(0805)	1 PCS	2242193110
68	R119	RES CF 4.7 K 1/8W +-5%	1 PCS	2222547011
69	R135	RES CuNi 10mΩ +-1%(錳銅線)	1 PCS	24911-0189
70	R111	RES MOF 43K 3W +-5% 立式(小型化)，不打KINK	1 PCS	2376543029
71	R125	RES W.W. 0.39 OHM 2W +-5% NKNP TYPE 立式 ，不打KINK	1 PCS	24735-398B
72	FOR C124	SRK TUBE 1φ*17mm	1 PCS	57701-0170
73	FOR CN101	RING TERMINAL *70mm	1 PCS	54B2310705
74	FOR PCB	SCREW M3*6 ISO/SW ZNC	2 PCS	6720530051
75	FOR Q101,D107,D106	SPRING SK-7	3 PCS	76455-0010
76	FOR CN101	SRK TUBE 5φ*0.9cm	1 PCS	57705-0090
77	FOR Q101,D107,D106	SRK TUBE 6φ*16mm	3 PCS	57706-0160
78	FOR C105	SRK TUBE 8φ*15mm	1 PCS	57708-0150
79	FOR R125	SRK TUBE 8φ*22mm	1 PCS	57708-0220
80	L101	Toroidal choke coil 2mH TN12.7*7.9*3.5(RD009)	1 PCS	45M36-502L
81	Q102	TR NPN 2SC4505 400V/0.1A (SMD)	1 PCS	14D2SC4505
82	Q103,Q105	TR NPN C2412K 50V/0.15A(SMD)	2 PCS	14C2C2412K
83	Q104	TR PNP A1037AK -50V/-0.15A(SMD)	1 PCS	14A21037AK
84	VAR101	VARISTOR SAS-471KD07 7φ	1 PCS	27111-0001
85	T101	X'FORMER PWR PQ2620 FOR CH-1205(RD010)	1 PCS	47S10-0040

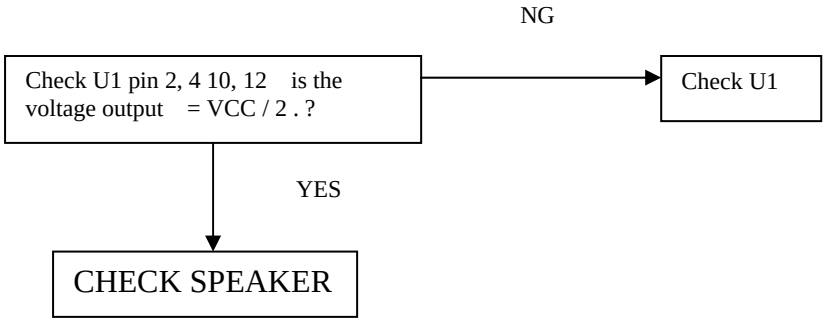
86	FOR FRONT HEATSINK	導熱墊片 TCR- 05 15*25-ASAHI	1 PCS	85011-0001
87	FOR FRONT HEATSINK	導熱墊片 TCR- 10 10*20-ASAHI	1 PCS	85100-0001
88		3M擋牆膠帶#44 1L 35*40mm	1 PCS	80400-0001
89		FRONT COVER 129.3*63.8*19.34mm	1 PCS	0810400020
90		BASE COVER 129.3*63.8*18.7mm	1 PCS	0820400020
91		DC OUTPUT POWER CABLE UL1185#18AWG φ5.5*φ2.5 *20.5,(音叉&車溝，黑)，L=80CM	1 PCS	56L1807811
92		FRONT HEATSINK FOR CH-1205	1 PCS	75170-0060
93		BOTTOM HEATSINK FOR CH-1205 REV:C	1 PCS	75170-005C
94		FRPP FOR CH-1205 BOTTOM HEATSINK	1 PCS	80300-0020
95		LED HOLDER 5*10	1 PCS	71720-0010
96		RATING FOR 捷聯 CH-1205 REV:C	1 PCS	0643C00026
97		15*4mm OK標籤 FOR 捷聯 CH-1205 REV:A	1 PCS	0643000031
98	FOR D106,D107	SILICON RUBBER COVER (TO-220ST-B)	2 PCS	80100-0001

6 D). AUDIO-MODULE Trouble shooting chart

I.) NO VOICE OUTPUT



II.) SOUND DISTORTION



AUDIO BOM

Bill Of Materials September 7,2001 18:09:14 Page1

Item	Quantity	Reference	Part
1	3	C1,C2,C4	1uF
2	1	C3	2200uF/25V
3	1	C5	10uF/50V
4	2	C6,C7	0.047uF
5	1	C8	100uF/16V
6	1	C9	100uF/25V
7	1	D1	LED
8	2	J1,J3	CON2
9	1	J2	EAR PHONE
10	1	J4	AUDIO IN
11	1	J5	DC IN
12	3	VR1,R1,R2	10K
13	1	R3	33K
14	1	R4	68K
15	2	R5,R6	15K
16	1	R7	130K
17	2	R9,R8	3K
18	2	R11,R10	1(3W)
19	1	R12	680
20	1	S1	SW SPST
21	1	U1	AN7522

GMZAN1

The gmZAN1device utilizes Genesis' patented third-generation Advanced Image Magnification technology as well as a proven integrated ADC/PLL to provide excellent image quality within a cost effective SVGA/XGA LCD monitor solution.
As a pin-compatible replacement for the gmB120, the gmZAN1 incorporates all of the gmB120 features plus many enhanced features; including 10-bit gamma correction, Adaptive Contrast Enhancement (ACE) filtering, Sync On Green (SOG), and an enhanced OSD.

1.1 Features

- Fully integrated 135MHz 8-bit triple-ADC, PLL, and pre-amplifier
- GmZ2 scaling algorithm featuring new Adaptive Contrast Enhancement (ACE)
- On-chip programmable OSD engine
- Integrated PLLs
- 10-bit programmable gamma correction
- Host interface with 1 or 4 data bits
- Pin-compatible with gmB120

Integrated Analog Front End

- Integrated 8-bit triple ADC
- Up to 135MHz sampling rates
- No additional components needed
- All color depths up to 24-bits/pixel are supported

High-Quality Advanced Scaling

- Fully programmable zoom
- Independent horizontal / vertical zoom
- Enhanced and adaptive scaling algorithm for optimal image quality
- Recovery Mode / Native Mode

Input Format

- Analog RGB up to XGA 85Hz
- Support for Sync On Green (SOG)
- Support for composite sync modes

Output Format

- Support for 8 or 6-bit panels (with high quality dithering)
- One or two pixel output format

Built In High-Speed Clock Generator

- Fully programmable timing parameters
- On-chip PLLs generate clocks for the on-chip ADC and pixel clock from a single reference oscillator

Auto-Configuration / Auto-Detection

- Phase and image positioning
- Input format detection

Operation Modes

- Bypass mode with no filtering
- Multiple zoom modes:
  - With filtering
  - With adaptive (ACE) filtering

Integrated On-Screen Display

- On-chip character RAM and ROM for better customization
- External OSD supported for greater flexibility
- Supports both landscape and portrait fonts
- Many other font capabilities including: blinking, overlay and transparency

1.3 Pin Description

Unless otherwise stated, unused input pins must be tied to ground, and unused output pins left open.

Table 1 : Analog-to-Digital Converter

PIN #	Name	I/O	Description
77	ADC_VDD2		Digital power for ADC encoding logic. Must be bypassed with 0.1uF capacitor to pin 78 (ADC_GND2)
78	ADC_GND2		Digital GND for ADC encoding logic. Must be directly connected to the digital system ground plane.
79	ADC_VDD1		Digital power for ADC clocking circuit. Must by passed with 0.1uF capacitor to pin 80 (ACD_GND1).
80	ADC_GND1		Digital GND for ADC clocking circuit. Must be directly connected to the digital system ground plane.
81	SUB_GNDA		Dedicated pin for substrate guard ring that protects the ADC reference system. Must be directly connected to the analog system ground plane.
82	ADC_GNDA		Analog ground for ADC analog blocks that are shared by all three channels. Includes bandgap reference, master biasing and full scale adjust. Must be directly connected to analog system ground plane.
84	ADC_VDDA		Analog power for ADC analog blocks that are shared by all three channels. Includes bandgap reference, master biasing and full scale adjust. Must be bypassed with 0.1uF capacitor to pin 82 (ADC_GNDA).
83	Reserved		For internal testing purpose only. Do not connect.
85	ADC_BGNDA		Analog ground for the blue channel. Must be directly connected to the analog system ground plane.
88	ADC_BVDDA		Analog power for the blue channel. Must be bypassed with 0.1uF capacitor to pin 85(BGNDA).
86	BLUE-	I	Negative analog input for the Blue channel.
87	BLUE+	I	Positive analog input for the Blue channel.
89	ADC_GGNDA		Analog ground for the green channel. Must be directly connected to the analog system ground plane.
92	ADC_GVDDA		Analog power for the green channel. Must be bypassed with 0.1uF capacitor to pin 89 (ADC_GGNDA).
90	GREEN-	I	Negative analog input for the Green channel.
91	GREEN+	I	Positive analog input for the Green channel.
93	ADC_RGNDA		Analog ground for the red channel. Must be directly connected to the analog system ground plane.
96	ADC_RVDDA		Analog power for the red channel. Must be bypassed with 0.1uF capacitor to pin 93 (ADC_RGNDA).
94	RED-	I	Negative analog input for the Red channel.
95	RED+	I	Positive analog input for the Red channel.

Table 2 : Host Interface (HIF) / External On-Screen Display

PIN #	Name	I/O	Description
98	HFS	I	Host Frame Sync. Frames the packet on the serial channel.
103	HCLK	I	Clock signal input for the 3-wire serial communication.
99	HDATA	I/O	Data signal for the 3-wire serial communication.
100	RESETn	I	Resets the gmZAN1 chip to a known state when low.
101	IRQ	O	Interrupt request output.
115	OSD-HREF	O	HSYNC output for an external OSD controller chip.
116	OSD-VREF	O	VSYNC output for an external OSD controller chip.
117	OSD-Clk	O	Clock output for an external OSD controller chip.
118	OSD-Data0	I	Data input 0 from an external OSD controller chip.
119	OSD-Data1	I	Data input 1 from an external OSD controller chip.
120	OSD-Data2	I	Data input 2 from an external OSD controller chip.
121	OSD-Data3	I	Data input 3 from an external OSD controller chip.
122	OSD-FSW	I	External OSD window display enable. Displays data from external OSD controller when high.
123	MFB11	I/O	Multi-Function Bus 11. One of twelve multi-function signals MFB[11:0].
124	MFB10	I/O	Multi-Function Bus 10. One of twelve multi-function signals MFB[11:0].
102	MFB9	I/O	Multi-Function Bus 9. One of twelve multi-function signals MFB[11:0]. Also used as HDATA3 in a 4-bit host interface configuration.
104	MFB8	I/O	Multi-Function Bus 8. One of twelve multi-function signals MFB[11:0]. Also used as HDATA2 in a 4-bit host interface configuration.
105	MFB7	I/O	Multi-Function Bus 7. One of twelve multi-function signals MFB[11:0]. Also used as HDATA1 in a 4-bit host interface configuration.
106	MFB6	I/O	Multi-Function Bus 6. One of twelve multi-function signals MFB[11:0]. Internally pulled up. When externally pulled down (sampled at reset) the host interface is configured for 4 bits wide. In this configuration, MFB9:7 are used as HDATA 3:1.
107	MFB5	I/O	Multi-Function Bus 5 One of twelve multi-function signals MFB[11:0]. Internally pulled up. When externally pulled down (sampled at reset) the chip uses an external crystal resonator across pins 141 and 142, instead of an oscillator.
109	MFB4	I/O	Multi-Function Bus 4. One of twelve multi-function signals MFB[11:0].
110	MFB3	I/O	Multi-Function Bus 3. One of twelve multi-function signals MFB[11:0].
111	FMB2	I/O	Multi-Function Bus 2. One of twelve multi-function signals MFB[11:0].
112	MFB1	I/O	Multi-Function Bus 1. One of twelve multi-function signals MFB[11:0].
113	MFB0	I/O	Multi-Function Bus 0. One of twelve multi-function signals MFB[11:0].

Table 3 : Clock Recovery / Time Base Conversion

PIN #	Name	I/O	Description
125	DVDD		Digital power for Destination DDS (direct digital synthesizer). Must be bypassed with a 0.1uF capacitor to digital ground plane.
127	DAC_DGNDA		Analog ground for Destination DDS DAC. Must be directly connected to the analog system ground plane.
128	DAC_DVDDA		Analog power for Destination DDS DAC. Must be bypassed with a 0.1uF capacitor to pin 127 (DAC_DGNDA).
129	PLL_DVDDA		Analog power for the Destination DDS PLL. Must be bypassed with a 0.1uF capacitor to pin 131 (PLL_DGNDA).
130	Reserved		For testing purposes only. Do not connect.
131	PLL_DGNDA		Analog ground for the Destination DDS PLL. Must be directly connected to the analog system ground plane.
132	SUB_DGNDA		Dedicated pin for the substrate guard ring that protects the Destination DDS. Must be directly connected to the analog system ground plane.
133	SUB_SGNDA		Dedicated pin for the substrate guard ring that protects the Source DDS. Must be directly connected to the analog system ground plane.
134	PLL_SGNDA		Analog ground for the Source DDS PLL. Must be directly connected to the analog system ground.
135	Reserved		For testing purposes only. Do not connect.
136	PLL_SVDDA		Analog power for the Source DDS DAC. Must be bypassed with a 0.1uF capacitor to pin 134 (PLL_SGNDA)
137	DAC_SVDDA		Analog power for the Source DDS DAC. Must be by passed with a 0.1uF capacitor to pin 138 (DAC_SGNDA)
138	DAC_SGNDA		Analog power for the Source DDS DAC. Must be directly connected to the analog system ground.
139	SVDD		Digital power for the Source DDS. Must be bypassed with a 0.1uF capacitor to digital ground plane.
141	TCLK	I	Reference clock(TCLK) input from the 50 MHz crystal oscillator
142	XTAL	O	If using an external oscillator, leave this pin floating. If using an external crystal, connect crystal between TCLK(141) and XTAL(142). See MFB5(pin 107).
143	PLL_RVDDA		Analog power for the Reference DDS PLL. Must be bypassed with a 0.1uF capacitor to pin 144(PLL_RGNDA)
144	PLL_RGNDA		Analog ground for the Reference DDS PLL. Must be directly connected to the analog system ground plane.
145	Reserved		For testing purposes only. Do not connect.
146	SUB_RGNDA		Dedicated pin for the substrate guard ring that protects the Reference DDS. Must be directly connected to the analog system ground plane.
148	VSYNC	I	CRT Vsync input. TTL Schmitt trigger input.
149	SYN_VDD		Digital power for CRT Sync input.
150	HSYNC/CSYNC	I	CRT Hsync or CRT composite sync input. TTL Schmitt trigger input.

Table 4. TFT Panel Interface

PIN #	Name	I/O	Description				
			2pxl/clk 8bit	2pxl/clk 6-bit	1pxl/clk 8-bit	1pxl/clk 6-bit	TFT
6	PD47	O	OB1	-	-	-	
7	PD46	O	OB0	-	-	-	
9	PD45	O	OG1	-	-	-	
10	PD44	O	OG0	-	-	-	
13	PD43	O	OR1	-	-	-	
14	PD42	O	OR0	-	-	-	
15	PD41	O	EB1	-	B1	-	
16	PD40	O	EB0	-	B0	-	
17	PD39	O	EG1	-	G1	-	
19	PD38	O	EG0	-	G0	-	
20	PD37	O	ER1	-	R1	-	
22	PD36	O	ER0	-	R0	-	
23	PD35	O	OB7	OB5	-	-	
24	PD34	O	OB6	OB4	-	-	
25	PD33	O	OB5	OB3	-	-	
26	PD32	O	OB4	OB2	-	-	
27	PD31	O	OB3	OB1	-	-	
28	PD30	O	OB2	OB0	-	-	
29	PD29	O	OG7	OG5	-	-	
31	PD28	O	OG6	OG4	-	-	
32	PD27	O	OG5	OG3	-	-	
34	PD26	O	OG4	OG2	-	-	
35	PD25	O	OG3	OG1	-	-	
36	PD24	O	OG2	OG0	-	-	
37	PD23	O	OR7	OR5	-	-	
38	PD22	O	OR6	OR4	-	-	
39	PD21	O	OR5	OR3	-	-	
42	PD20	O	OR4	OR2	-	-	
46	PD19	O	OR3	OR1	-	-	
47	PD18	O	OR2	OR0	-	-	
48	PD17	O	EB7	EB5	B7	B5	
50	PD16	O	EB6	EB4	B6	B4	
51	PD15	O	EB5	EB3	B5	B3	
52	PD14	O	EB4	EB2	B4	B2	
53	PD13	O	EB3	EB1	B3	B1	
54	PD12	O	EB2	EB0	B2	B0	
55	PD11	O	EG7	EG5	G7	G5	
56	PD10	O	EG6	EG4	G6	G4	
57	PD9	O	EG5	EG3	G5	G3	
62	PD8	O	EG4	EG2	G4	G2	

PIN #	Name	I/O	Description 2pxl/clk 8bit	2pxl/clk 6-bit	1pxl/clk 8-bit	1pxl/clk 6-bit	TFT
63	PD7	O	EG3	EG1	G3	G1	
64	PD6	O	EG2	EG0	G2	G0	
66	PD5	O	ER7	EG5	R7	R5	
67	PD4	O	ER6	ER4	R6	R4	
68	PD3	O	ER5	ER3	R5	R3	
69	PD2	O	ER4	ER2	R4	R2	
70	PD1	O	ER3	ER1	R3	R1	
71	PD0	O	EG2	ER0	R2	R0	
43	PdispE	O	This output provides a panel display enable signal that is active when flat panel data is valid.				
74	PHS	O	This output provides the panel line clock signal.				
73	PVS	O	This output provides the frame start signal.				
44	PCLKA	O	This output is used to drive the flat panel shift clock.				
45	PCLKB	O	Same as PCLKA above. The polarity and the phase of this signal are independently programmable.				
75	Pbias	O	This output is used to turn on/off the panel bias power or controls backlight.				
76	Ppwr	O	This output is used to control the power to a flat panel.				

Table 5. Test Pins

PIN #	Name	I/O	Description
3	PSCAN	I	Enable automatic PCB assembly test. When this input is pulled high, the automatic PCB assembly test mode is entered. An internal pull-down resistor drives this input low for normal operation.
155	SCAN_IN1	I	Scan input 1 used for automatic PCB assembly tesing.
157	SCAN_IN2	I	Scan input 2 used for automatic PCB assembly tesing.
159	SCAN_OUT1	O	Scan output 1 used for automatic PCB assembly tesing.
160	SCAN_OUT2	O	Scan output 2 used for automatic PCB assembly tesing.
153	Reserved		
154	Reserved		

Table 6. VDD / VSS for Core Circuitry, Host Interface, and Panel/Memory Interface

PIN #	Description
65, 40, 33, 12	PVDD4~PVDD1 for panel / memory interface. Connect to +3.3V. Must be the same voltage as the CVDD's
149, 108, 58, 21, 11	SRVDD2-1, CVDD4, CVDD2-1 for core circuitry. Connect to +3.3V. Must be the same voltage as the PVDD's.
158, 151, 140, 126, 114, 72, 61, 49, 41, 30, 18, 8, 1	Digital grounds for core circuiry and panel / memory interface.

1.4 System-level Block Diagram

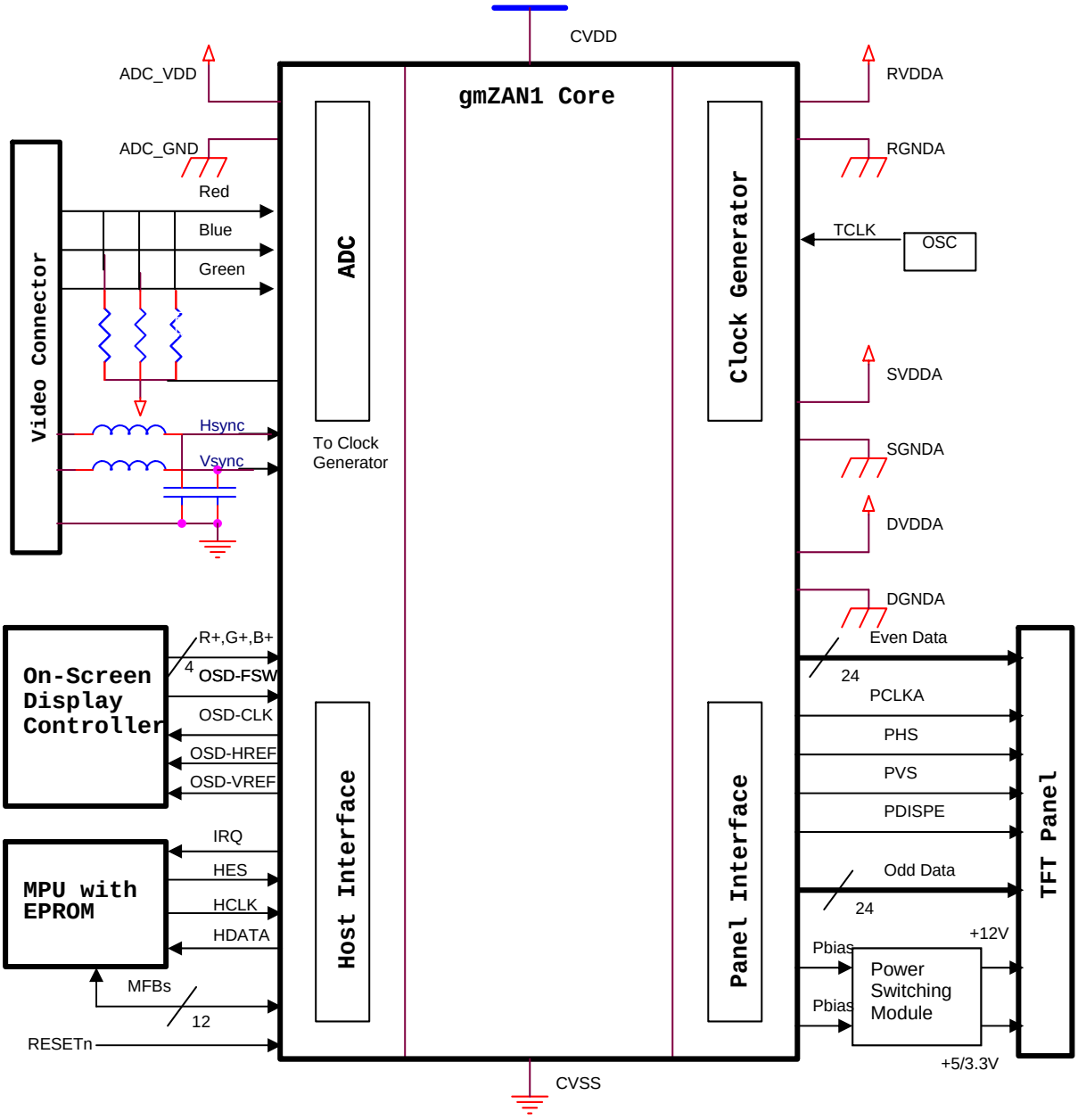


Figure 2. Typical Stand-alone Configuration

1.5 Operating Modes

The Source Clock (also called SCLK in this document) and the Panel Clock are defined as follows:

- The Source Clock is the sample clock regenerated from the input Hsync timing (called clock recovery) by SCLK DDS (direct digital synthesis) and the PLL.
- The Panel Clock is the timing clock for panel data at the single pixel per clock rate. The actual PCLK to the panel may be one-half of this frequency for double-pixel panel data format. When its frequency is different from that of source clock, the panel clock is generated by Destination Clock (or DCLK) DDS/PLL.

There are six display modes: Native, Slow DCLK, Zoom, Downscaling, Destination Stand Alone, and Source Stand Alone.
Each mode is unique in terms of:

- Input video resolution vs. panel resolution
- Source Clock frequency / Panel Clock frequency ratio
- Source Hsync frequency / Panel Hsync frequenc ratio
- Data source (analog RGB, panel background color, on-chip pattern generator

1.5.1 Native

Panel Clock frequency = Source Clock frequency
Panel Hsync frequency = Input Hsync frequency
Panel Vsync frequency = Input Vsync frequency

This mode is used when the input resolution is the same as the panel resolution and the input data clock frequency is within the panel clock frequency specification of the panel being used.

1.5.2 Slow DCLK

Panel Clock frequency < Source Clock frequency
Panel Hsync frequency = Input Hsync frequency
Panel Vsync frequency = Input Vsync frequency

This mode is used when the input resolution is the same as the panel resolution, but the input data clock frequency is exceeds the panel clock frequency specification of the panel being used. The panel clock is scaled to the Source Clock, and the internal data buffers are used to spread out the timing of the input data by making use of the large CRT blanking time to extends the panel horizontal display time.

1.5.3 Zoom

Panel Clock frequency > Source Clock frequency
Panel Hsync frequency > Input Hsync frequency
Panel Vsync frequency = Input Vsync frequency

This mode is used when the input resolution is less than the panel resolution. The input data clock is then locked to the pnael clock, which is at a higher frequency. The input data is zoomed to the panel resolution.

1.5.4 Downscaling

Panel Clock frequency < Source Clock frequency
Panel Hsync frequency < Input Hsync frequency
Panel Vsync frequency = Input Vsync frequency

This mode is used when the input resolution is greater than the panel resolution, to provide enough of a display to enable the user to recover to a supported resolution. The input clock is operated at a frequency less than that of the input pixel rate(under-sampled horizontally) and the scaling filter is used to drop input lines. In this mode, zoom scaling must be disabled

1.5.5 Destination Stand Alone

Panel Clock = DCLK in open loop (not locked)
Panel Hsync frequency = DCLK frequency / (Destination Htotal register value)
Panel Vsync frequency = DCLK frequency / (Dest. Htotal register value * Dest. Vtotal register value)

This mode is used when the input is changing or not available. The OSD may still be used as in all other display modes and stable panel timing signals are produced. This mode may be automatically set when the gmZAN1 detects input timing changes that could cause out- of-spec operation of the panel.

1.5.6 Source Stand Alone

Panel Clock = DCLK in open loop (not locked to input Hsync)
Panel Hsync frequency = SCLK frequency / (Source Htotal register value)
Panel Vsync frequency = SCLK frequency / (Source Htotal register value *Source Vtotal register value)

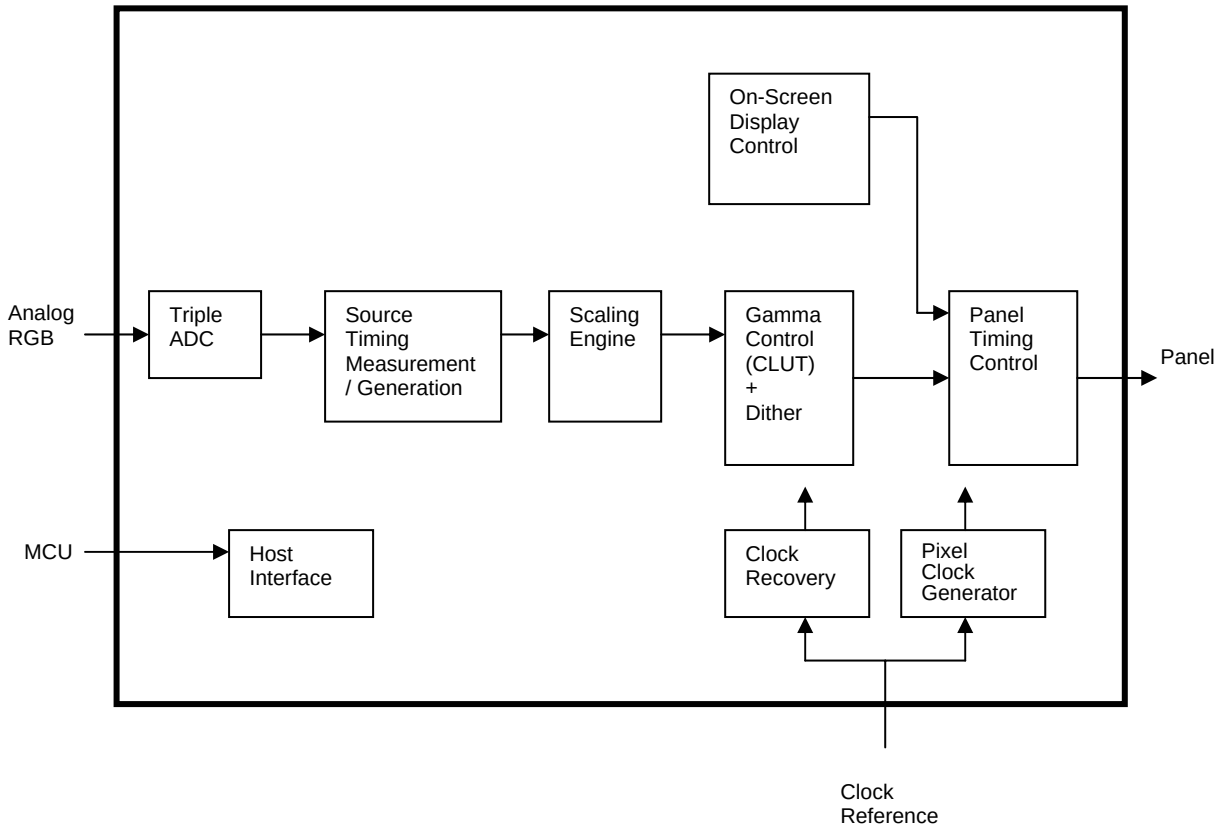
This mode is used to display the pattern generator data. This mode may be useful for testing an LCD panel on the manufacturing line (color temperature calibration, etc.).

2. FUNCTIONAL DESCRIPTION

Figure 3 below shows the main functional blocks inside the gmZAN1

2.1 Overall Architecture

Figure 3. Block Diagram for gmZAN1



2.2 Clock Recovery Circuit

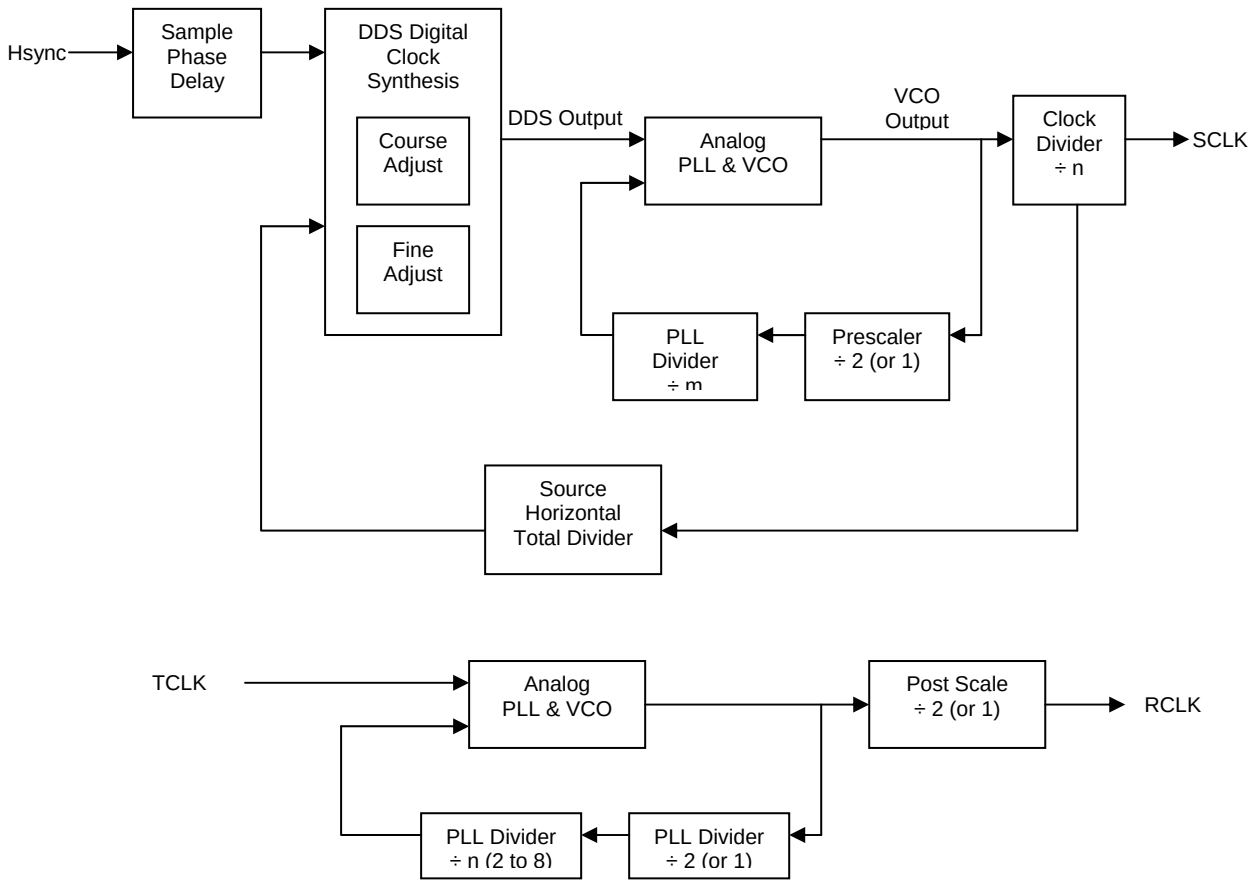
The gmZAN1 has a built-in clock recovery circuit. This circuit consists of a digital clock synthesizer and an analog PLL. The clock recovery circuit generates the clock used to sample analog RGB data (SCLK or source clock). This circuit is locked to the HSUNC of the incoming video signal. The RCLK generated from the TCLK input is used as a reference clock.

The clock recovery circuit adjusts the SCLK period so that the feedback pulse generated every SCLK period multiplied by the Source Horizontal Total value (as programmed into the registers) locks to the rising edge of the Hsync input. Even though the initial SCLK frequency and the final SCLK frequency are as far apart as 60MHz , locking can be achieved in less than 1ms across the operation voltage/temperature range.

The SCLK frequency (1/SCLK period) can be set to the range of 10-to-135 MHz. Using the DDS (direct digital synthesis) technology the clock recovery circuit can generate any SCLK clock frequency within this range.

The pixel clock (DCLK or destination clock) is used to drive a panel when the panel clock is different from SCLK (or SCLK/2). It is generated by a circuit virtually identical to the clock recovery circuit. The difference is that DCLK is locked to SCLK while SCLK is locked to the Hsync input. DCLK frequency divided by N is locked to SCLK frequency divided by M. The value M and N are calculated and programmed in the register by firmware. The value M should be close to the Source Htotal value.

Figure 4. Clock Recovery Circuit



The table below summarizes the characteristics of the clock recovery circuit.

Table 7. Clock Recovery Characteristics

	Minimum	Typical	Maximum
SCLK Frequency	10MHz		135 MHz
Sampling Phase Adjustment		0.5 ns/step, 64 steps	

Patented digital clock synthesis technology makes the gmZAN1 clock circuits very immune to temperature/voltage drift.

2.2.1 Sampling Phase Adjustment

The ADC sampling phase is adjusted by delaying the Hsync input at the programmable delay cell inside the gmZAN1. The delay value can be adjusted in 64 steps, 0.5 ns/step. The accuracy of the sampling phase is checked by the gmZAN1 and the "score" can be read in a register. This feature will enable accurate auto-adjustment of the ADC sampling phase.

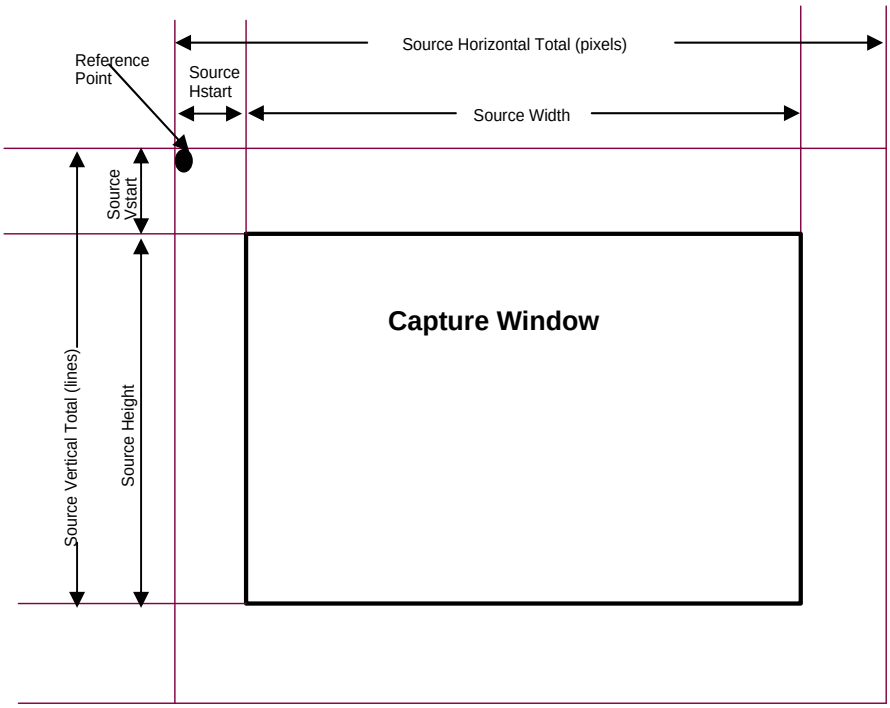
2.2.2 Source Timing Generator

The STG module defines a capture window and sends the input data to the data path block. The figure below shows how the window is defined.
For the horizontal direction, it is defined in SCLKs (equivalent to a pixel count). For the vertical direction, it is defined in lines.
All the parameters in the figure that begin with "Source" are programmed into the gmZAN1 registers.
Note that the vertical total is solely determined by the input.
The reference point is as follows:

- The first pixel of a line: the pixel whose SCLK rising edge sees the transition of the HSYNC polarity from low to high.
- The first line of a frame: the line whose HSYNC rising edge sees the transition of the VSYNC polarity from low to high.

The gmZAN1 also supports the use of analog composite sync and digital sync signals as described in Section 2.3.2

Figure 5. Capture Window



2.3 Analog-to-Digital Converter

2.3.1 Pin Connection

The RGB signals are to be connected to the gmZAN1 chip as described in Table 8 and Table 9.

Table 8. Pin Connection for RGB Input with Hsync/Vsync

GmZAN1 Pin Name (Pin Number)	CRT Signal Name
Red+(#95)	Red
Red- (#94)	N/A (Tie to Analog GND for Red on the board)
Green+(#91)	Green
Green- (#90)	N/A (Tie to Analog GND for Green on the board)
Blue+(#87)	Blue
Blue- (#86)	N/A (Tie to Analog GND for Blue on the board)
HSYNC/CS (#150)	Horizontal Sync
VSYNC (#148)	Vertical Sync

Table 9. Pin Connection for RGB Input with Composite Sync

GmZAN1 Pin Name (Pin Number)	CRT Signal Name
Red+(#95)	Red
Red- (#94)	N/A (Tie to Analog GND for Red on the board)
Green+(#91)	Green When using Sync-On-Green this signal also carries the sync pulse.
Green- (#90)	N/A (Tie to Analog GND for Green on the board)
Blue+(#87)	Blue
Blue- (#86)	N/A (Tie to Analog GND for Blue on the board)
HSYNC/CS (#150)	Digital composite sync. Not applicable for Sync-On-Green

The gmZAN1 chip has three ADC's (analog-to-digital converters), one for each color (red, green, and blue). Table 10 summarizes the characteristics of the ADC.

Table 10. ADC Characteristics

	MIN	TYP	MAX	NOTE
RGB Track & Hold Amplifiers				
Band Width		160MHz		
Settling Time to 1/2%		8.5ns		Full Scale Input = 0.75V, BW=160MHz(*)
Full Scale Adjust Range @ R,G,B Inputs	0.45V		0.95V	
Full Scale Adjust Sensitivity		+/-1 LSB		Measured @ ADC Output (**)
Zero Scale Adjust Range				For a larger DC offset from an external video source, the AC coupling feature is used to remove the offset.
Zero Scale Adjust Sensitivity		+/-1 LSB		Measured @ ADC Output
ADC+RGB Track & Hold Amplifiers				
Sampling Frequency (fs)	20MHz		110MHz	
DNL			+/- 0.9LSB	fs = 80 MHz
INL		+/- 1.5LSB		fs = 80 MHz
Channel to Channel Matching		+/- 0.5LSB		
Effective Number of Bits (ENOB)		7 Bits		fin = 1MHz, fs=80 MHz Vin= -1db below full scale=0.75V
Power Dissipation		400mW		fs=110 MHz, Vdd=3.3V
Shut Down Current			100uA	

(*) Guaranteed by design (**) Independent of full scale R,G,B input

The gmZAN1 ADC has a built-in clamp circuit. By inserting series capacitors (about 10 nF) the DC offset of an external video source can be removed. The clamp pulse position and width are programmable.

2.3.2 Sync. Signal Support

The gmZAN1 chip supports digital separate sync (Hsync/Vsync), digital composite sync, and analog composite sync (also known as sync-on-green). All sync types are supported without external sync separation / extraction circuits.

Digital Composite Sync
The types of digital composite sync inputs supported are:
- OR/AND type: No Csync pulses toggling during the vertical sync period
- XOR type: Csync polarity changes during the vertical sync period

The gmZan1 provides enough sync status information for the firmware to detect the digital composite sync type.

Sync-On-Green (Analog Composite Sync)
The voltage level of the sync tip during the vertical sync period can be either –0.3V or 0V

2.3.3 Display Mode Support

A mode calculation utility (MODECALC.EXE) provided by Genesis Microchip may be run before compilation of the firmware to determine which input modes can be supported. Refer to firmware documents for more details.

2.4 Input Timing Measurement

As described in section 2.2.2 above, input data is sent from the analog-to-digital converter to the source timing generator (STG) block. The STG block defines a capture window (Figure5).

The input timing measurement block consists of the source timing measurement (STM) block and interrupt request (IRQ) controller. Input timing parameters are measured by the STM block and stored in registers. Some input conditions will generate an IRQ to an external micro-controller. The IRQ generating conditions are programmable.

2.4.1 Source Timing Measurement

When it receives the active CRT signal (R,G,B and Sync signals) the Source Timing Measurement unit begins measuring the horizontal and vertical timing of the incoming signal using the sync signals and TCLKi as a reference. Horizontal measurement occurs by measuring a minimum and a maximum value for each parameter to account for TCLKi sampling granularity. The measured value is updated every line. Vertical parameters are measured in terms of horizontal lines. The trailing edge of the Hsync input is used to check the polarity of the Vsync input.
The table below lists all the parameters that may be read in the source timing measurement (STM) registers of the gmZAN1.

Table 11. Input Timing Parameters Measured by the STM Block

Parameter	Unit	Updated at:
HSYNC Missing	N/A	Every 4096 TCLKs and every 80ms (2-bits)
VSYNC Missing	N/A	Every 80ms
HSYNC/VSYNC Timing Change	N/A	When the horizontal period delta or the vertical period delta to the previous line / frame exceeds the threshold value (programmable).
HSYNC Polarity	Positive/Negative	After register read
VSYNC Polarity	Positive/Negative	Every frame
Horizontal Period Min/Max	TCLKs and SCLKs	After register read
HSYNC High Period Min/Max	TCLKs	After register read
Vertical Period	Lines	Every frame
VSYNC High Period	Lines	Every frame
Horizontal Display Start	SCLKs	Every frame
Horizontal Display End	SCLKs	Every frame
Vertical Display Start	Lines	Every frame
Vertical Display End	Lines	Every frame
Interlaced Input Detect	N/A	Every frame
CRC Data/Line Data	N/A	Every frame
CSYNC Detect	N/A	Every 80ms

The display start/end registers store the first and the last pixels/lines of the last frame that have RGB data above a programmed threshold.
The reference point of the STM block is the same as that of the source timing generator (STG) block:

- The first pixel: the pixel whose SCLK rising edge sees the transition of the HSYNC polarity from low to high.
- The first line: the line whose HSYNC rising edge sees the transition of the VSYNC polarity from low to high.

The CRC data and the line data are used to detect a test pattern image sent to the gmZAN1 input port.

2.4.2 IRQ Controller

Some input timing conditions can cause the gmZAN1 chip to generate an IRQ. The IRQ-generating conditions are programmable, as given in the following table.

Table 12. IRQ-Generation Conditions

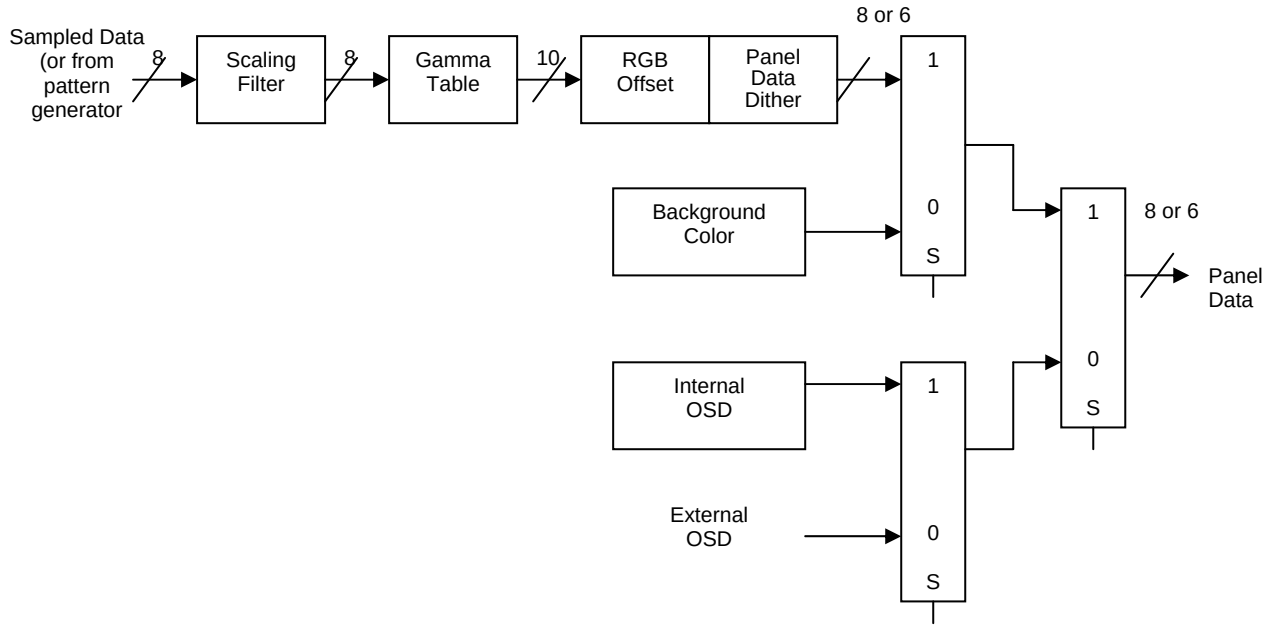
IRQ Event	Remark
Timing Event	One of the three events: ● Leading edge of Vsync input, ● Panel line count (the line count is programmable), ● Every 10ms Only one event may be selected at a time.
Timing Change	Any of the following timing changes: ● Sync loss, ● DDS tracking error beyond threshold, ● Horizontal/vertical timing change beyond threshold Threshold values are programmable.

Reading the IRQ status flags will not affect the STM registers.
Note that if a new IRQ event occurs while the IRQ status register is being read, the IRQ signal will become inactive for minimum of one TCLK period and then get re-activated. The polarity of the IRQ signal is programmable.

2.5 Data Path

The data path block of gmZAN1 is shown in Figure 6.

Figure 6. gmZAN1 Data Path



2.5.1 Scaling Filter

The gmZAN1 scaling filter uses an advanced adaptive scaling technique proprietary to Genesis Microchip Inc. and provides high quality scaling of real time video and graphics images. This is Genesis' third generation scaling technology that benefits from the expertise and feedback gained by supporting a wide range of solutions and applications.

2.5.2 Gamma Table

The gamma table is used to adjust the RGB data for the individual display characteristics of the TFT panel. The overall gamma of the display may be set, as well as separate corrections for each of the three display channels. In addition, the gamma table may be used for contrast, brightness, and white balance (temperature) adjustments. The lookup table has an 8-bit input (256 different RGB entries) and produces a 10-bit output.

2.5.3 RGB Offset

The RGB offsets provide a simple shift (positive or negative) for each of the three color channels. This may be used as a simple brightness adjustment within a limited range. The data is clamped to zero for negative offsets, and clamped to FFh for positive offsets. This adjustment is much faster than recalculating the gamma table, and could be used with the OSD user controller to provide a quick brightness adjust. An offset range of plus 127*4 to minus 127*4 is available.

2.5.4 Panel Data Dither

For TFT panels that have fewer than eight bits for each R,G,B input, the gmZAN1 provides ordered and random dithering patterns to help smoothly shade colors on 6-bit panels.

2.5.5 Panel Background Color

A solid background color may be selected for a border around the active display area. The background color is most often set to black.

2.6 Panel Interface

The gmZAN1 chip interfaces directly with all of today's commonly used active matrix flat panels with 640x480, 800x600 and 1024x768 resolutions. The resolution and the aspect ratio are NOT limited to specific values.

2.6.1 TFT Panel Interface Timing Specification

The TFT panel interface timing parameters are listed in Table 13 below. Refer to three timing diagrams of Figure 7 and Figure 8 for the timing parameter definition. All aspects of the gmZAN1 interface are programmable. For horizontal parameters, Horizontal Display Enable Start, Horizontal Display Enable End, Horizontal Sync Start and Horizontal Sync End are programmable. Vertical Display Enable Start, Vertical Display Enable End, Vertical Sync Start and Vertical Sync End are also fully programmable.
In order to maximize panel data setup and hold time, the panel clock (PCLKA, PCLKB) output skew is programmable. In addition, the current drive strength of the panel interface pins is programmable.

Table 13. gmZAN1 TFT Panel Interface Timing

Signal Name			**Min**	**Typical**	**Max**	**Unit**
PVS	Period	t1	0	16.67	2048 -	lines ms
	Frequency			60	-	Hz
	Front porch	t2	0		2048	lines
	Back porch	t3	0		2048	lines
	Pulse width	t4	0		2048	lines
	PdispE	t5	0	Panel height	2048	lines
	Disp. Start from VS	t6	0		2048	lines
	PVS set up tp PHS	t18	1		2048	PCLK *1
	PVS hold from PHS	t19	1		2048	PCLK *1
PHS	Period	t7	0		2048 [1024	PCLK *1
	Front porch	t8	0		2048	PCLK *1
	Back porch	t9	0		2048	PCLK *1
	Pulse width	t10	0		2048	PCLK *1
	PdispE	t11	0	Panel width	2048 [1024]	PCLK *1
	Disp. Start fom HS	t12	0		2048	PCLK *1
PCLKA, PCLKB*4	Frequency	t13			120 [60]	MHz
	Clock (H) *2	t14	DCLK/2-3 [DCLK-3]		DCLK/2-2 [DCLK-2]	ns
	Clock (L) *2	t15	DCLK/2-3 [DCLK-3]		DCLK/2-2 [DCLK-2]	ns
	Type		-	One pxl/clock [two pxl/clock]	-	
Data	Set up *3	t16	DCLK/2-5 [DCLK-5]		DCLK/2-2 [DCLK-2]	ns
	Hold *3	t17	DCLK/2-5 [DCLK-5]		DCLK/2-2 [DCLK-2]	ns
	width		3 bits	18 bits [36 bits]	24 bits [48 bits]	bits/pixel

NOTE: Numbers in [ ] are for two pixels/clock mode.

NOTE: The drive current of the panel interface signals is programmable as shown in Table 1. The drive current is to be programmed through the API upon chip initialization. Output current is programmable from 2 mA to 20mA in increments of 2 mA. Drive strength should be programmed to match the load presented by the cable and input of the panel. Values shown are based on a loading of 20pF and a drive strength of 8 mA.

NOTE *1: The PCLK is the panel shift clock.

NOTE *2: The DCLK stands for Destination Clock (DCLK) period. Is equal to:

-PCLK period in one pixel/clock mode,

-twice the PCLK period in two pixels/clock mode.

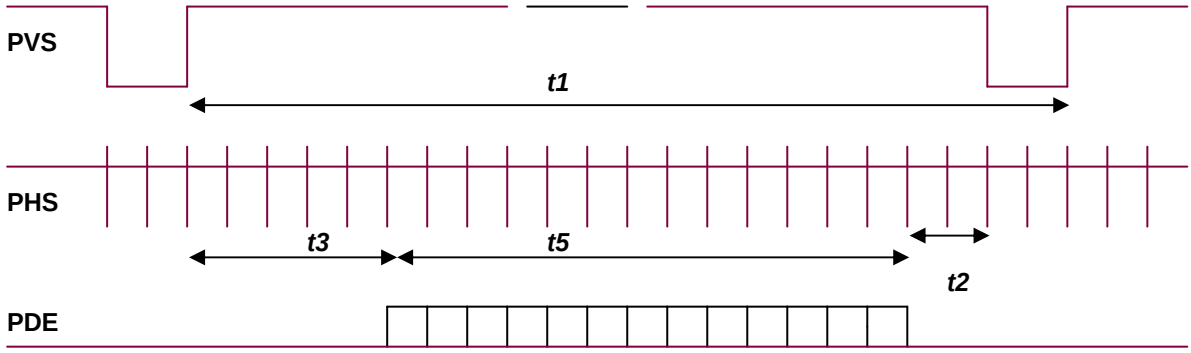
NOTE *3: The setup/hold time spec. for PCLK also applies to PHS and PdispE. The setup time (t16) and the hold time (t17) listed in this table are for the case in which no clock-to-data skew is added. The PVS/PHS/PdispE/Pdata signals are asserted on the rising edge of the PCLK. The polarity of the PCLK and its skew are programmable. Clock to Data skew can be adjusted in sixteen 800-ps increments. In combination with the PCLK polarity inversion, the clock-to-data phase can be adjusted in total of 31 steps.

NOTE *4: The polarity of the PCLKA and the PCLKB are independently programmable.

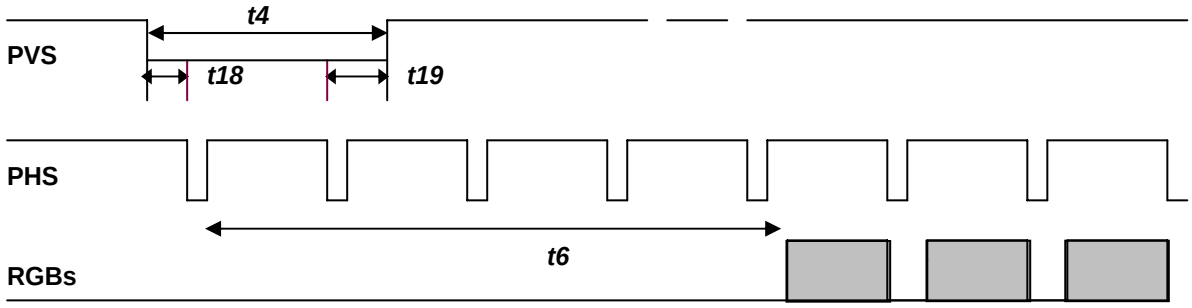
The micro controller must have all the timing parameters of the panel used for the monitor. The parameters are to be stored in a non-volatile memory. As can be seen from this table, the wide range of timing programmability of the gmZAN1 panel interface makes it possible to support various kinds of panels known today:

Figure 7. timing Diagrams of the TFT Panel Interface (One pixel per clock)

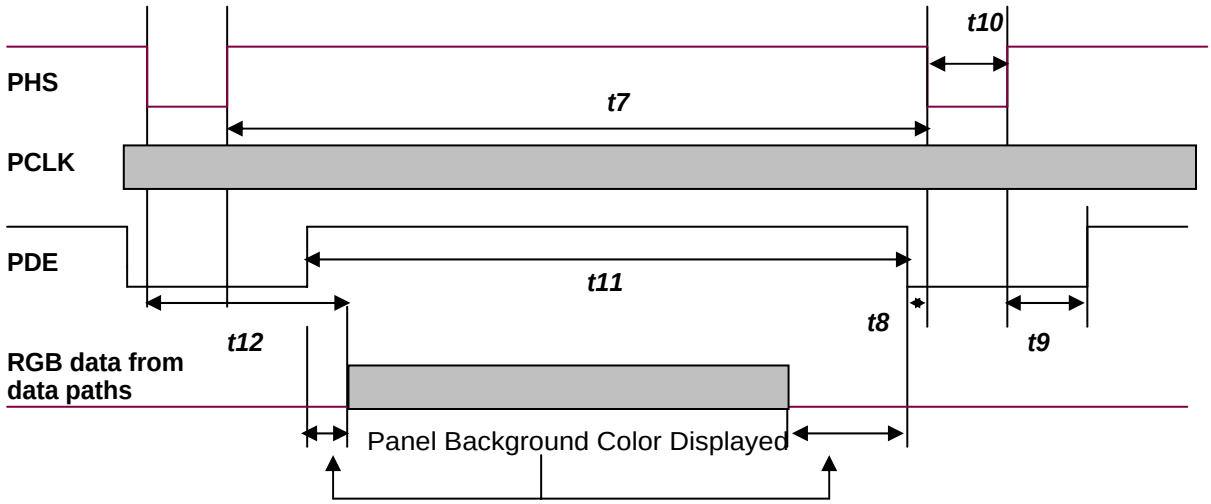
(a) Vertical size in TFT



(b) Vsync width and display position in TFT



(c) Horizontal size in TFT



(d) Hsync width in TFT

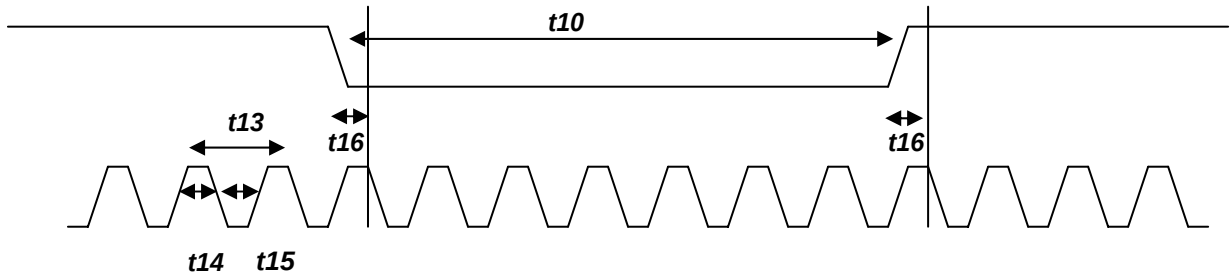
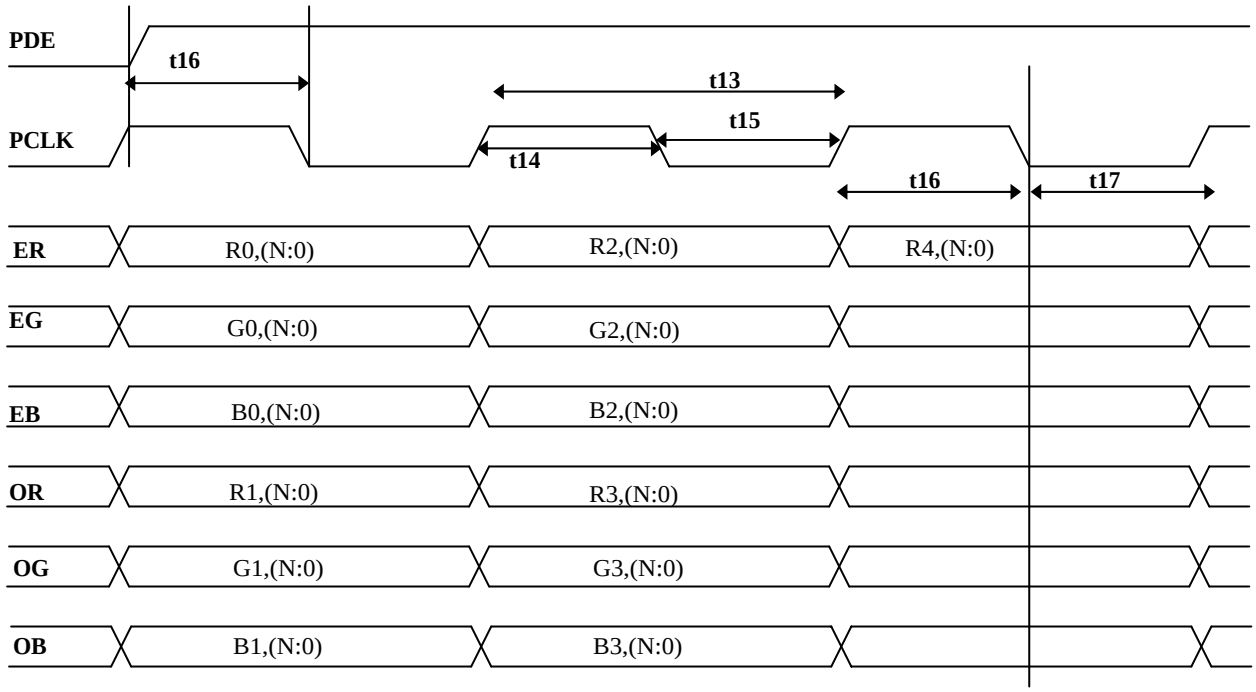
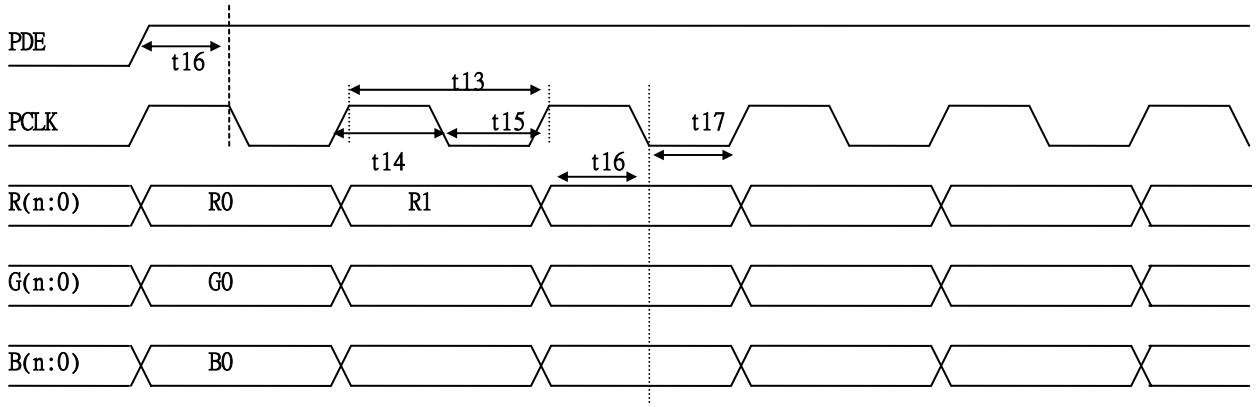


Figure 8. Data latch timing of the TFT Panel Interface

(a) Two pixel per clock mode in TFT



(b) One pixel per clock mode in TFT



2.6.2 Power Manager

LCD panels require logic power, panel bias power, and control signals to be sequenced in a specific order, otherwise severe damage may occur and disable the panel permanently. The gmZAN1 has a built in power sequencer (Power Manager) that prevents this kind of damage.
The Power Manager controls the power up/down sequences for LCD panels within the four states described below. See the timing diagram Figure 9.

2.6.2.1 State 0 (Power Off)

The Pbias signal and Ppower signal are low (inactive). The panel controls and data are forced low. This is the final state in the power down sequence. PM is kept in state 0 until the panel is enabled.

2.6.2.2 State 1 (Power On)

Intermediate step 1. The Ppower is high (active), the Pbias is low (inactive), and the panel interface is forced low (inactive).

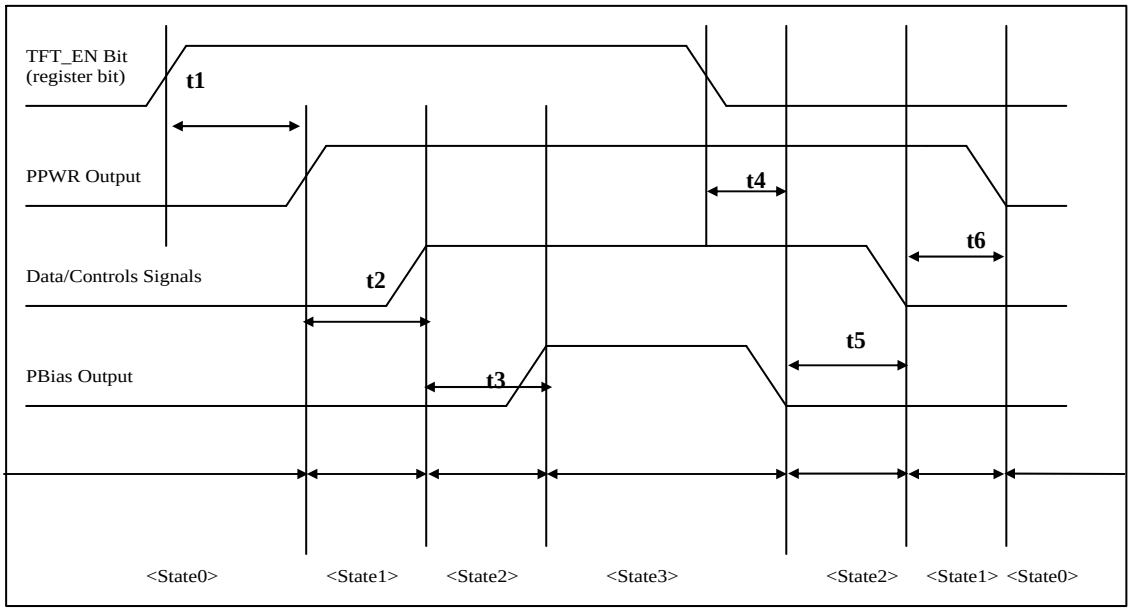
2.6.2.3 State 2 (Panel Drive Enabled)

Intermediate step 2. The Ppower is high (active), the Pbias is low (inactive), and the panel interface is active.

2.6.2.4 State 3 (Panel Fully Active)

This is the final step in the power up sequence, with Ppower and Pbias high (active), and the panel interface active. PM is kept in this state until the internal TFT_Enable signal controlled by Panel Control register is disabled. The panel can be disabled through either an API call under program control or automatically by the gmZAN1 to prevent damage to the panel.

Figure 9. Panel Power Sequence



In Figure 9 above, t2=t6 and t3=t5. t1,t2,t3 and t4 are independently programmable from one to eight steps in length. The length of each step is in the range of 511 * X* (TCLKi cycle) or (TCLKi cycle) * 32193 *X, where X is any positive integer value equal to or less than 256. TCLKi is the reference clock to the gmZAN1 chip, and ranges from 14.318 MHz to 50 MHz in frequency. This programmability provides enough flexibility to meet a wide range of power sequencing requirements by various panels.

2.6.3 Panel Interface Drive Strength

As mentioned previously, the gmZAN1 has programmable output pads for the TFT panel interface. Three groups of panel interface pads (panel clock, data, and control) are independently controllable and are programmed using API calls. See the API reference manual for details.

Table 14. Panel Interface Pad Drive Strength

Value (4 bits)	Drive Strength in mA
0	Outputs are in tri-state condition
1	2mA
2	4mA
3	6mA
4	8mA
5	10mA
6	12mA
7	14mA
8	16mA
9	18mA
10,11,12,13,14,15	20mA

2.7 Host Interface

The host microcontroller interface of the gmZAN1 has two modes of operation: gmB120 compatible mode, and a 4-bit serial interface mode.

- GmB120 compatible mode-Four signals consisting of 1 data bit, a frame synchronization signal, a clock signal and an Interrupt Request signal (IRQ). This mode is entered when a pull-down resistor is not connected to MFB6(pin number 106).
- 4-bit serial interface mode-Same as gmB120 compatible mode with the addition of three data bits so that four data bits are transferred on each clock edge. This mode is entered when a (10K ohm) pull-down resistor is connected to MFB6(pin number 106).

When the chip is configured for 4-bit host interface, MFB9:7 are used as HDATA3:1 and HDATA is used as HDATA0. For instruction, Read Data, or Write Data, the data order is D3:0, D7:4, D11:8, The burst mode operation then uses three clocks (instead of twelve) for each 12-bit data (or address) transmission.

In both modes, a reset pin sets the chip to a known state when the pin is pulled low. The RESETn pin must be low for at least 100ns after the CVDD has become stable (between +3.15V and +3.45V) in order to reset the chip to a known state.

The gmZAN1 chip has an on-chip pull-down resistor in the HFS input pad. No external pull-up is required. The signal stays low until driven high by the microcontroller.

2.7.1 Serial Communication Protocol

In the serial communication between the microcontroller and the gmZAN1, the microcontroller always acts as an initiator while the gmZAN1 is always the target. The following timing diagram describes the protocol of the serial channel of the gmZAN1 chip.

Figure 10. Timing Diagram of the gmZAN1 Serial Communication

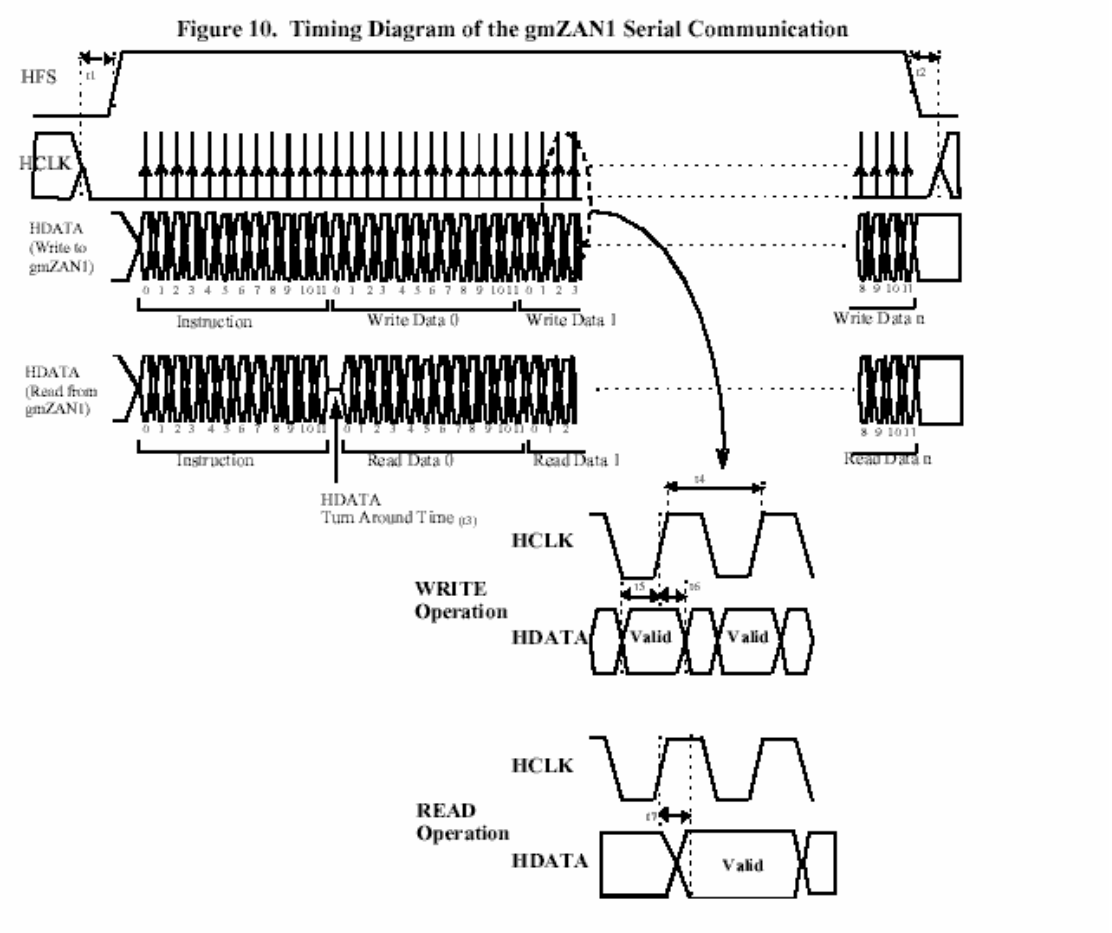


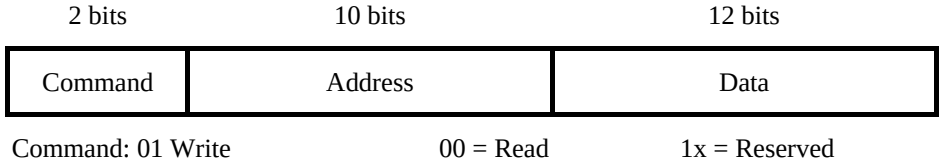
Table 15 summarizes the serial channel specification of the gmZAN1. Refer to Figure 10 for the timing parameter definition.

Table 15. gmZAN1 Serial Channel Specification

Parameter	Min.	Typ.	Max.
Word Size (Instruction and Data)	---	12 bits	---
HCLK low to HFS high (t1)	100 ns		
HFS low to HCLK inactive (t2)	100 ns		
HDATA Write to Read Turnaround Time (t3)	1 HCLK cycle		1 HCLK cycle
HCLK cycle (t4)	100 ns		
Data in setup time (t5)	25 ns		
Data in hold time (t6)	25 ns		
Data out valid (t7)	5 ns		10

In the read operation, the microcontroller (Initiator) issues an instruction lasting 12 HCLKs. After the last bit of the command is transferred to the gmZAN1 on the 12th clock, the microcontroller must stop driving data before the next rising edge of HCLK at which point the gmZAN1 will start driving data. At the 13th rising edge of HCLK, the gmZAN1 will begin driving data.

Figure 11. Serial Host Interface Data Transfer Format



Note that when the chip is configured for a 4-bit host interface, MFB9:7 are used as HDATA 3:1 and HDATA is used as HDATA0. The command and address information are transferred as Address 1:0+Command1:0, Address5:2 and Address9:6. The data information is transferred as Data3:0,Data 7:4, Data 11:8. Thus, in this mode the HDATA pin carries Command0, Address2, Address6, Data0, Data4 and Data8.
On the gmZAN1 reference design board, the microcontroller toggles the HCLK and HDATA lines under program control. Genesis Microchip provides API calls to facilitate communication between the microcontroller and the gmZAN1. Refer to the API reference manual for details.

2.7.2 Multi-Function Bus (MFB)

The Multi-Function Bus provides additional 12 pins that are used as general purpose input and output (GPIO) pins. Each pin can be independently configured as input or output.
MFB pins 9 through 5 have special functions:

- When a 10K ohm pull-down resistor is connected to MFB6 (MFB6 has an internal pull-up resistor) MFB9:7 are used as host data bits HDATA3:1.
- When a 10K ohm pull-down resistor is connected to MFB5 (MFB5 has an internal pull-up resistor) a crystal can be placed between XTAL and TCLK instead of using an external oscillator for the TCLK input.

Note that all pins on the multi-function bus MFB11:0 are internally pulled-up.

2.8 On-Screen Display Control

The gmZAN1 chip has a built-in OSD (On-Screen Display) controller with an integrated font ROM. The chip also supports an external OSD controller for monitor vendors to maintain a familiar user interface.
The internal and external OSD windows may be displayed anywhere the panel Display Enable is active, regardless of whether the panel would otherwise display panel background color or active data.

2.8.1 OSD Color Map

Both the internal and external OSD display use a 16 location SRAM block for the color programming. Each color location is a twelve-bit value that defines the upper four bits of each of the 8 bit Red, Blue and Green color components as follows:

- D3:0 Blue; D7:4 of blue component of color
- D7:4 Green; D7:4 of green component of color
- D11:8 Red; D7:4 of red component of color

To extend the 4-bit color value programmed to the full 8 bits the following rule is applied: if any of the upper four color bits are a "1", then R (G, B) data 3:0=1111b, otherwise R (G, B) data 3:0=0000b

2.8.2 On-Chip OSD Controller

The internal OSD uses a block of SRAM of 1536x12 bits and a ROM of 1024x12 bits. The SRAM is used for both the font data and the character-codes while the ROM is used to store the bit data for 56 commonly used characters. The font data is for 12 pixel x 18 line characters, one bit per pixel. The font data starts at address zero. The character-codes start at any offset (with an address resolution of 16) that is greater than the last location at which font data has been written . It is the programmer's responsibility to ensure that there is no overlap between fonts and character-codes. This implementation results in a trade-off between the number of unique fonts on-screen at any one time and the total number of characters displayed. For example, one configuration would be 98 font maps (56 fonts in ROM and 42 fonts in SRAM) and 768 characters (e.g. in a 24x32 array).

The on-chip OSD of the gmZAN1 can support a portrait mode (in which the LCD monitor screen is rotated 90 degrees). In this portrait mode, all the fonts must be loaded in the SRAM, because the ROM stores fonts for a landscape mode (typical orientation) only. The font size in the portrait mode is 12 pixels by 12 lines. As is the case in landscape mode, the SRAM is divided into a font storage area and a character code storage area. For example, 64 fonts can be stored in RAM and an OSD window of 768 characters (such as 24x32) can still be displayed.

The first address of SRAM to be read for the first character displayed (upper left corner of window)is also programmable, with an address resolution of 16 (8-bits as the top bits of the 12-bit SRAM address). The character-code is a 12-bit value used as follows:

- D6:0 font-map select, this is the top seven bits of the address for the first line of font bits
- D8:7 Background color, 00=bcolor0, 01=bcolor1, 10=bcolor2, 11=transparent background
- D10:9 Foreground color (0, 1, 2 or 3)
- D11 Blink enable if set to 1, otherwise no blink

Although the OSD color map has room for sixteen colors, only seven are used by the internal OSD: three background colors and four foreground colors.

The blink rate is based on either a 32 or 64 frame cycle and the duty cycle may be selected as 25/75/50/50% or 75/25%. The 2-bit foreground and background attributes directly select the color (there is no indirect "look-up", i.e. there is no TMASK function). The 2560 addresses of the ROM/SRAM are mapped as 10 segments of 256 contiguous addresses each, to the OSD memory page of 100h-1FFh in the host interface. A 4-bit register value selects the segment to map to the host R/W page.

The character cell height and width are programmable from 5-66 pixels or 2-65 lines. The X/Y offset of the font bit-map upper-left pixel relative to the upper-left pixel of the character cell is also programmable from 0-63 (pixels or lines). The OSD window height and width in characters/rows is programmable from 1-64.

The Start X/Y position for the upper left corner of the OSD window is programmable (in panel pixels and lines) from 0-2047. There is an optional window border (equal width on all four sides of the window) or a window shadow (the window bottom and right side) the border is a solid color that is selected by an SRAM location as RGB444. The border width may be set as 1, 2, 4 or 8 pixels/lines. These parameters are summarized in Figure 12 and Table 16.
The Font Data D11:0 for each line is displayed with bit D11 first (leftmost) and D0 last.
The reference point for the OSD start is always the upper left corner of the Panel display, which is the start (leading edge) of Panel Display Enable for both Horizontal and Vertical timing.

The OSD Window start position sets the location of the first pixel of the OSD to display, including any border. That is; if the border is enabled, the start of the character display of the OSD is offset from the OSD start position by the width/height of the border.

To improve the appearance and make it easy to find the OSD window on the screen, the user may select optional shadowing (3D effect). The “Shadow” feature operates in the same manner as in the B120; that is, it produces a region of half intensity (scaler data) pixels of the same width and height as the OSD window, but offset to the right and down by 8 pixels/lines (the border width setting has no effect). OSD foreground and background colors always cover the OSD window region of the “shadow”, but transparent background pixels in the OSD will show the half intensity panel data. Therefore, it is not recommended to use both the “shadow” feature and transparent background OSD pixels together. The ”shadow” does not change the intensity of any panel background color over which it may be located. The border and shadow are mutually exclusive, only one may be selected at a time.

The OSD window is not affected by the scaling operation. The size will stay the same whether the source input data is scaled or not.

2.9 TCLK Input

The source timing is measured by using the TCLK input as a reference. Also, the reference clock to the on-chip PLLs are derived from the TCLK. It is therefore crucial to have a jitter-free clock reference.
Table 19 shows the requirements for the TCLK signal.

Table 19. TCLK Specification

Frequency	20 MHz to 50 MHz
Jitter	250 ps maximum
Rise Time (10% to 90%)	5 ns
Duty Cycle	40-60

There is also an option to use a crystal (instead of an oscillator) for the TCLK input. This option is selected by pulling down MFB5 and connecting the crystal between XTAL and TCLK.

3. ELECTRICAL CHARACTERISTICS

Table 20. Absolute Ratings

Parameter	Min.	Typ.	Max.	Note
PVDD			5.6 volts	
CVDD			5.6 volts	
Vin	Vss-0.5 volt		Vcc+0.5V	
Operating temperature	0 degree C		70 degree C	
Storage temperature	-65 degree C		150 degree C	
Maximum power consumption			~2W	

Table 21. DC Electrical Characteristic

Parameter	Min.	Typ.	Max.	Note
PVDD	3.15 volts	3.3 volts	3.47 volts	
CVDD	3.15 volts	3.3 volts	3.47 volts	
Vil (COMS inputs) Vil (TTL inputs)			0.3*CVDD 0.8 volts	
Vih (COMS inputs) Vih (TTL inputs)	0.7 * CVDD 2.0 volts		1.1*CVDD 5.0+0.5 volts	(1)
Voh	2.4 volts		CVDD	
Vol		0.2 volts	0.4 volts	
Input Current	-10 uA		10 uA	
PVDD operating supply current	0 mA		20 mA/pad @ 10pF	(2)
CVDD operating supply current	0 mA		500 mA	(3)

NOTE 1:5V-Tolerent TTL Input pads are as follows:

- CRT Interface: HSYNC (pin #150), VSYNC (#148)
- Host Interface: HFS (#98), HCLK (#103), HDATA (#99), RESETN (#100), MFB[11:0]: MFB11 (#123), MFB10 (#124), MFB9 (#102), MFB8 (#104), MFB7 (#105), MFB6 (#106), MFB5 (#107), MFB4 (#109), MFB3 (#110), MFB2 (#111), MFB1 (#112), MFB0 (#113)
- OSD Interface: OSD_DATA3 (#121), OSD_DATA2 (#120), OSD_DATA1 (#119), OSD_DATA0 (#118), OSD_FSW (#122)
- Non-5V-Tolerant TTL Input Pad is: TCLK(#141)

NOTE 2: When the panel interface is disabled, the supply current is 0 mA. The drive current of each pad can be programmed in the range of 2 mA to 20 mA (@capacitive loading = 10 pF)

NOTE 3: When all circuits are powered down and TCLK is stopped, the CVDD supply current becomes 0 mA.

7. MECHANICAL OF CABINET FRONT DIS-ASSEMBLY

For temporary, this page still not available.

Wait for mechanical drawing !

PARTS LIST OF CABINET

LOCATION	T780KMGHBAA0A	SPECIFICATION
	AUPC780A1	17” LCD AUDIO BOARD
	CBPC780GM	17” CONVERSION BOARD
	DCPC780A3	17” DC POWER BOARD
	KEPC780EK	KEYBOARD

12A	381	1				RUBBER FOOT
15A	5684	1				MAIN FRAME
15A	5689	1				GND.CABLE CLAMP
15A	5689	2				GND. CLAMP
26A	800	13				LCD BAR-CODE
33A	3647	1				POWER LED LENS
33A	4058	Y	L			POWER KEY PAD
33A	4060	Y	L			CABLE COVER
33A	4061	Y	L			AUDIO POWER BUTTON
33A	4062	Y	L			VOLUME KNOB
33A	4063	Y	L			SCREW COVER
34A	756	1Y	L			FRONT PANEL (AOC)
34A	757	Y	1L			BACK COVER
34A	758	Y	L			SUPPORT FRONT (AUDIO)
34A	759	Y	3L			SUPPORT BACK
34A	760	Y	L			BASE
34A	761	Y	L			ARM COVER
37A	443	1				LCD HINGE
40A	155	237				ID LABEL (LM-700A)
41A	401	948	1A			OWNERS MANUAL
44A	3147	1				WOODEN FLAT PALLES 1140X1
44A	3148	1				WOODEN FLAT PALLES 1140X1
44A	3234	1				EPS CUSHION (L)
44A	3234	2				EPS CUSHION (R)
44A	3234	5				CARTON (AOC)
44A	3253	1				BASE SHEET
45A	113	1				PE BAG
45A	114	1				PE BAG
45A	116	1				CLIP BAG
52A	1208	A				ALUMINIUM TAPE 35X25
52A	194	1				50CM X 500MX X 0.017MMt
70A	L17	3A0C				DRIVER DISK
78A	309	1				SPEAKER 16 OHM 2W 30* 70
79A	L17	1	S			INVERTER BY SAMPO
80A	L17	2	C		H	ADAPTOR WHITE
85A	548	3				SHIELD CBPC
85A	574	1				SHIELD INVERTER
85A	583	1				SOFT-SHIELD
85A	583	6				SOFT-SHIELD
85A	583	7				SOFT-SHIELD
85A	583	8				SOFT-SHIELD
89A	173	56	4			AUDIO CABLE
89A	174D	5BFG	L		F	SIGNAL CABLE
89A	404C	18N	I		S	POWER CORD
95A	8013	2	29			HARNESS 2P 75mm
95A	8014	5	5A			HARNESS
95A	8018	30	1			HARNESS
B1A	1030	5128				SCREW 3X5mm
B1A	1030	5128				SCREW 3X5 mm
B1A	1030	8128				SCREW 3X8mm
B1A	1030	8128				SCREW 3X8 mm
M1A	330	6128				SCREW M3X6mm
M1A	330	6128				SCREW M3X6mm
M1A	330	6128				SCREW M3X6mm
M1A	1030	10128				SCREW M3X10mm
M1A	1740	12128				SCREW M4X12mm
Q1A	330	8120				SCREW 3X8mm
Q1A	340	12128				SCREW 4X12mm
Q1A	340	16128				SCREW 4X16mm

PARTS LIST OF CABINET (continue)

LOCATION	T780KMGHBAA0A	SPECIFICATION
Q1A	1030 10128	SCREW
Q1A	1030 12128	SCREW 3X12mm
Q1A	1030 12128	SCREW 3X12mm
750A	LCD 170 3	LCD-PANEL M170E1-01 BY CHI-MEI

PARTS LIST OF CONVERSION BOARD

LOCATION	CBPC780GM				SPECIFICATION
CN303	33A	3802-	5H		WAFER 5P RIGHT ANELE PITCH 2.0
CN302	33A	3802-	9H		WAFER 9P RIGHT ANELE PITCH 2.0
CN602	33A	3802-	10H		WAFER 10P RIGHT ANELE PITCH
CN601	33A	3802-	14H		WAFER 14P RIGHT ANELE PITCH
R319	33A	8009-	2 -		2 PIN MIN. JUMPER
JP201	33A	8009-	3		3 PIN PLUG
JP303	33A	8009-	3		3 PIN PLUG
	33A	8810-	2	L	2P SHUNT MINI JUMPER
CN200	33A	8013-	14	H	PLUG 14P 90
	40A	152-	43		LABEL (CBPC780GM)
	44A	3231-	8		EVA
U302	56A	1125-	61	M	M6759FG BY ALI
C307	67A	305-	331	6	330uF +- 20% 35V
C309	67A	305-	331	6	330uF +- 20% 35V
C310	67A	305-	331	6	330uF +- 20% 35V
C312	67A	305-	331	6	330uF +- 20% 35V
C927	67A	305-	331	6	330uF +- 20% 35V
C928	67A	305-	331	6	330uF +- 20% 35V
C945	67A	309-	471	3T	470uF +- 20% 16V
FB301	71A	55-	28		BEAD P6H 7.62*5.08*6.4 BY TEC
T300	73A	253-	108	Y	CHOKE COIL BY SHINING
T300	73A	253-	108	LI	CHOKE COIL BY LINEARITY
L905	73A	259-	4		200UH +/-5%
VR501	75A	335-	103		10K OHM +-30% RH0615C14J ALPS
	90A	372-	2		HEAT SINK
X300	93A	22-	55		CRYSTAL 20MHz HC-49US
U201	93A	22-	57		OSCILLATOR 50MHz –3.3V
CN301	95A	9001-	6A		HARNESS

LOCATION	AI780GM				SPECIFICATION
U601	56A	561-	5		NT7181 56L TSSOP
U602	56A	561-	5		NT7181 56L TSSOP
U200	56A	562-	8		gmZAN1 PQFP-160 GENESIS
U304	56A	563-	1		CHIP LM2596S- 5.0 BY NS
U305	56A	563-	7		AIC1084-33M TO-263 ANALOG
U202	56A	566-	6		CHIP SI9953DY-T1 SILICON
U904	56A	585-	2		LT1117 SMD SOT223 BY LINEARITY
U904	56A	585-	4		AIC1117-33CY SOT-223 ANALOG
U401	56A	74F-	14		CHIP MC74F14 BY MOTOROLA
U401	56A	74F-	14	P	N74F14D BY PHILIPS
U203	56A	1133-	16		CHIP 24LC21A/SN BY MICRO
U300	56A	1133-	17		AT24C04N-10SC BY ATMEL
U300	56A	1133-	29		24LC04BT/SC SOI18 MICRO
Q200	57A	417-	4		CHIP PMBS3904 BY PHILIPS
Q304	57A	417-	4		CHIP PMBS3904 BY PHILIPS
D303	57A	754-	1		BAT54C-GS08 SOT-23 TELEFUKON
D303	57A	754-	2		BAT54C
RP300	61A	125-	103 -	8	CHIP ARRAY 10K OHM 1/16W 8P4R
L207	61A	0603-	000		CHIP 0 OHM 1/16W
R200	61A	0603-	000		CHIP 0 OHM 1/16W
R201	61A	0603-	000		CHIP 0 OHM 1/16W
R202	61A	0603-	000		CHIP 0 OHM 1/16W
R203	61A	0603-	000		CHIP 0 OHM 1/16W
R207	61A	0603-	000		CHIP 0 OHM 1/16W
R208	61A	0603-	000		CHIP 0 OHM 1/16W
R229	61A	0603-	000		CHIP 0 OHM 1/16W
R317	61A	0603-	000		CHIP 0 OHM 1/16W
R340	61A	0603-	000		CHIP 0 OHM 1/16W
R603	61A	0603-	000		CHIP 0 OHM 1/16W
R905	61A	0603-	000		CHIP 0 OHM 1/16W
R218	61A	0603-	101		CHIP 100 OHM 1/16W
R219	61A	0603-	101		CHIP 100 OHM 1/16W
R220	61A	0603-	101		CHIP 100 OHM 1/16W
R227	61A	0603-	101		CHIP 100 OHM 1/16W
R213	61A	0603-	102		CHIP 1KOHM 1/16W
R214	61A	0603-	102		CHIP 1KOHM 1/16W
R216	61A	0603-	103		CHIP 10K OHM 1/16W
R217	61A	0603-	103		CHIP 10K OHM 1/16W
R223	61A	0603-	103		CHIP 10K OHM 1/16W
R224	61A	0603-	103		CHIP 10K OHM 1/16W
R225	61A	0603-	103		CHIP 10K OHM 1/16W
R300	61A	0603-	103		CHIP 10K OHM 1/16W
R301	61A	0603-	103		CHIP 10K OHM 1/16W
R311	61A	0603-	103		CHIP 10K OHM 1/16W
R313	61A	0603-	103		CHIP 10K OHM 1/16W
R315	61A	0603-	103		CHIP 10K OHM 1/16W
R326	61A	0603-	103		CHIP 10K OHM 1/16W
R327	61A	0603-	103		CHIP 10K OHM 1/16W
R328	61A	0603-	103		CHIP 10K OHM 1/16W
R329	61A	0603-	103		CHIP 10K OHM 1/16W
R209	61A	0603-	202		CHIP 2K OHM 1/16W
R210	61A	0603-	202		CHIP 2K OHM 1/16W
R204	61A	0603-	750		CHIP 75 OHM 1/16W
R205	61A	0603-	750		CHIP 75 OHM 1/16W
R206	61A	0603-	750		CHIP 75 OHM 1/16W
C229	65A	0603-	103 -	32	CHIP 0.01UF 50V X7R
C230	65A	0603-	103 -	32	CHIP 0.01UF 50V X7R
C231	65A	0603-	103 -	32	CHIP 0.01UF 50V X7R
C232	65A	0603-	103 -	32	CHIP 0.01UF 50V X7R
C233	65A	0603-	103 -	32	CHIP 0.01UF 50V X7R
C234	65A	0603-	103 -	32	CHIP 0.01UF 50V X7R
C251	65A	0603-	103 -	32	CHIP 0.01UF 50V X7R
C606	65A	0603-	103 -	32	CHIP 0.01UF 50V X7R
C608	65A	0603-	103 -	32	CHIP 0.01UF 50V X7R
C614	65A	0603-	103 -	32	CHIP 0.01UF 50V X7R

LOCATION	AI780GM					SPECIFICATION
C616	65A	0603-	103 -	32		CHIP 0.01UF 50V X7R
C201	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C202	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C204	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C205	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C207	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C208	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C209	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C210	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C211	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C212	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C213	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C215	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C217	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C218	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C219	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C220	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C221	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C222	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C223	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C225	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C226	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C227	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C228	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C237	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C244	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C245	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C246	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C300	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C304	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C308	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C311	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C405	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C601	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C602	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C604	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C618	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C619	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C939	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C940	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C941	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C942	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C944	65A	0603-	104 -	12		CHIP 0.1UF 16V X7R
C250	65A	0603-	330 -	31		CHIP33PF 50V NPO
C303	65A	0603-	330 -	31		CHIP 33PF 50V NPO
C306	65A	0603-	330 -	31		CHIP 33PF 50V NPO
CP301	65A	600M-	102 -	8T		CHIP ARRAY 1000PF 8P
CP302	65A	600M-	102 -	8T		CHIP ARRAY 1000PF 8P
C605	67A	312-	100 -	3		SMD EC 10UF 16V 85C B
C607	67A	312-	100 -	3		SMD EC 10UF 16V 85C B
C613	67A	312-	100 -	3		SMD EC 10UF 16V 85C B
C615	67A	312	100	3	1	SMD EC 10UF 16V 85C B
C620	67A	312	100	3	1	SMD EC 10UF 16V 85C B
C200	67A	312	101	3	1	SMD EC 100UF 16V 85C D
C203	67A	312	101	3	1	SMD EC 100UF 16V 85C D
C206	67A	312	101	3	1	SMD EC 100UF 16V 85C D
C214	67A	312	101	3	1	SMD EC 100UF 16V 85C D
C216	67A	312	101	3	1	SMD EC 100UF 16V 85C D
C224	67A	312	101	3	1	SMD EC 100UF 16V 85C D
C305	67A	312	101	3	1	SMD EC 100UF 16V 85C D
C403	67A	312	101	3	1	SMD EC 100UF 16V 85C D

LOCATION	AI780GM					SPECIFICATION
C603	67A	312	101	3	1	SMD EC 100UF 16V 85C D
C943	67A	312	101	3	1	SMD EC 100UF 16V 85C D
C313	67A	312	220	3	1	SMD EC 22UF 16V 85C CSIZE
C314	67A	312	220	3	1	SMD EC 22UF 16V 85C CSIZE
L200	71A	57G	601		1	CHIP BEAD 600 OHM 1206 T13216
L201	71A	57G	601		1	CHIP BEAD 600 OHM 1206 T13216
L202	71A	57G	601		1	CHIP BEAD 600 OHM 1206 T13216
L203	71A	57G	601		1	CHIP BEAD 600 OHM 1206 T13216
L300	71A	57G	601		1	CHIP BEAD 600 OHM 1206 T13216
L900	71A	57G	601		1	CHIP BEAD 600 OHM 1206 T13216
L601	71A	59B	121		1	CHIP BEAD 120 OHM 0603 TB1608
L602	71A	59B	121		1	CHIP BEAD 120 OHM 0603 TB1608
L603	71A	59B	121		1	CHIP BEAD 120 OHM 0603 TB1608
L604	71A	59B	121		1	CHIP BEAD 120 OHM 0603 TB1608
R215	71A	59B	121		1	CHIP BEAD 120 OHM 0603 TB1608
L601	71A	59C	121	B	0	CHIP BEAD 120 OHM 0603 FCM160
L602	71A	59C	121	B	0	CHIP BEAD 120 OHM 0603 FCM160
L603	71A	59C	121	B	0	CHIP BEAD 120 OHM 0603 FCM160
L604	71A	59C	121	B	0	CHIP BEAD 120 OHM 0603 FCM160
R215	71A	59C	121	B	0	CHIP BEAD 120 OHM 0603 FCM160
MTG U3	87A	202	44		1	IC SOCKET 44P PLCC
D200	93A	391	39		1	CHIP ZD 5.6V BY FCI MLL752
D201	93A	391	39		1	CHIP ZD 5.6V BY FCIMLL752
D208	93A	391	39		1	CHIP ZD 5.6V BY FCI MLL752
D209	93A	391	39		1	CHIP ZD 5.6V BY FCIMLL752
D210	93A	391	39		1	CHIP ZD 5.6V BY FCIMLL752
D200	93A	391	47		0	ZENER DIODES TZMC5V6-GS8
D201	93A	391	47		0	ZENER DIODES TZMC5V6-GS8
D208	93A	391	47		0	ZENER DIODES TZMC5V6-GS8
D209	93A	391	47		0	ZENER DIODES TZMC5V6-GS8
D210	93A	391	47		0	ZENER DIODES TZMC5V6-GS8
D200	93A	391	49		0	CHIP ZD 5.6V BY FULL POWMLL523
D201	93A	391	49		0	CHIP ZD 5.6V BY FULL POWMLL523
D208	93A	391	49		0	CHIP ZD 5.6V BY FULL POWMLL523
D209	93A	391	49		0	CHIP ZD 5.6V BY FULL POWMLL523
D210	93A	391	49		0	CHIP ZD 5.6V BY FULL POWMLL523
D300	93A	602	11		1	SMB340 BY FULL POWER
D300	93A	602	12		0	SMB340 BY FCI
D300	93A	602	12		0	SMB340 BY FCI
D202	93A	64	32		1	LL4148 SMD BY FCI
D203	93A	64	32		1	LL4148 SMD BY FCI
D204	93A	64	32		1	LL4148 SMD BY FCI
D205	93A	64	32		1	LL4148 SMD BY FCI
D206	93A	64	32		1	LL4148 SMD BY FCI
D207	93A	64	32		1	LL4148 SMD BY FCI
D301	93A	64	32		1	LL4148 SMD BY FCI
D302	93A	64	32		1	LL4148 SMD BY FCI
D202	93A	64	32	U	0	MLL4148 SMD BY FULL POWER
D203	93A	64	32	U	0	MLL4148 SMD BY FULL POWER
D204	93A	64	32	U	0	MLL4148 SMD BY FULL POWER
D205	93A	64	32	U	0	MLL4148 SMD BY FULL POWER
D206	93A	64	32	U	0	MLL4148 SMD BY FULL POWER
D207	93A	64	32	U	0	MLL4148 SMD BY FULL POWER
D301	93A	64	32	U	0	MLL4148 SMD BY FULL POWER
D302	93A	64	32	U	0	MLL4148 SMD BY FULL POWER
D202	93A	64	32	V	0	LL4148 GS08 SMD BY VISHAY
D203	93A	64	32	V	0	LL4148 GS08 SMD BY VISHAY
D204	93A	64	32	V	0	LL4148 GS08 SMD BY VISHAY
D205	93A	64	32	V	0	LL4148 GS08 SMD BY VISHAY
D206	93A	64	32	V	0	LL4148 GS08 SMD BY VISHAY
D207	93A	64	32	V	0	LL4148 GS08 SMD BY VISHAY
D301	93A	64	32	V	0	LL4148 GS08 SMD BY VISHAY
D302	93A	64	32	V	0	LL4148 GS08 SMD BY VISHAY
	715A	820	3		1	TF1780 MAIN BOARD 125 X 13

PARTS LIST OF KEY PC BOARD

LOCATION	KEPC780EK				Quantity	SPECIFICATION
TP101	9A	308	1			PIN
TP102	9A	308	1			PIN
J7	33A	3252	3		H	WAFER 3P 3.96mm 90
	40A	152	44			LABEL (KEPC780EK)
Q101	57A	419	PP	T		
Q102	57A	419	PP	T		
R101	61A	6021	0352	T		10K OHM 5% 1/6W
R102	61A	6021	0352	T		10K OHM 5% 1/6W
R103	61A	6021	0352	T		10K OHM 5% 1/6W
R104	61A	6021	0352	T		10K OHM 5% 1/6W
R105	61A	6021	0352	T		10K OHM 5% 1/6W
R106	61A	6021	0352	T		10K OHM 5% 1/6W
R107	61A	6021	0352	T		10K OHM 5% 1/6W
R108	61A	6022	2152	T		220 OHM 5% 1/6W
C101	65A	450	104	7T		0.1Uf+80-20% 56V Y5V
SW1	77A	600	1	G		TACT SWITCH
SW2	77A	600	1	G		TACT SWITCH
SW3	77A	600	1	G		TACT SWITCH
SW4	77A	600	1	G		TACT SWITCH
SW5	77A	600	1	G		TACT SWITCH
LED1	81A	13	1	B	H	LED 5*7 mmBL-RYG202N
JP2	88A	304	1	S		DC POWER JACK SCD-014A BY SC
J101	95A	90	23			TIN COATED
	95A	8014	9	6	A	HARNESS
	715A	778	1			KEPC-1780F LCD K/B

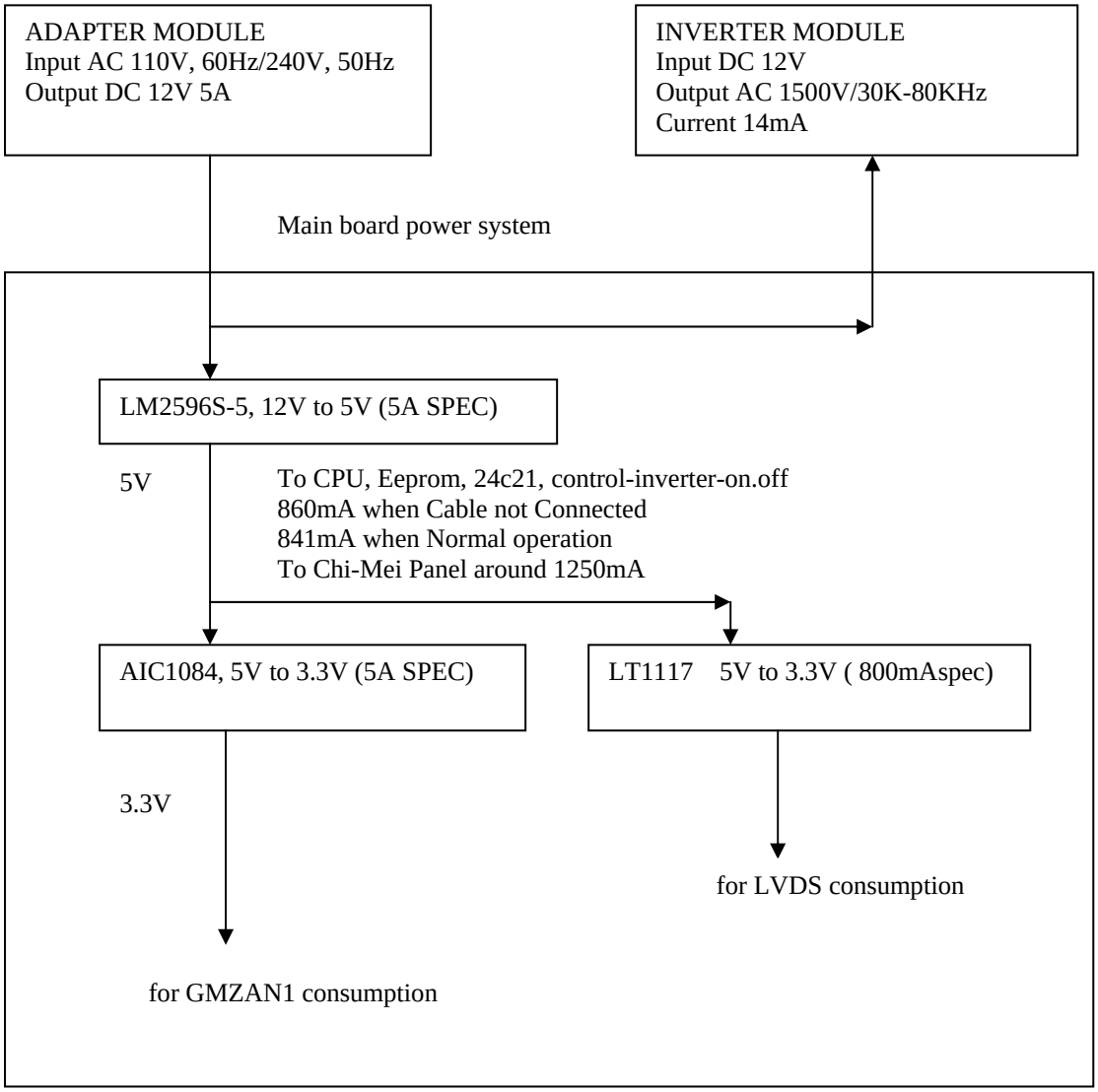
PARTS LIST OF DC-POWER BOARD

LOCATION	DCPC780A3				Quantity	SPECIFICATION
P4	33A	3278	2		1	2P PLUG B2B-XHA/JST B2B-XHA/JS
P3-1	33A	3278	3		1	3P PLUG B3B-XHA/JST B3B-XHA/JS
C71	67A	305	331	6	1	330uF+－ 20% 35V
J2	88A	302	4	S	1	3.5mm P JACK SCJ-0356A-B-X SC
J1	88A	304	1	S	1	DC POWER JACK SCD-014A BY SC
JP3	89A	171	27	A	1	DC POWER CORD
	715A	851	2		1	LCD USB & AUDIO BRD

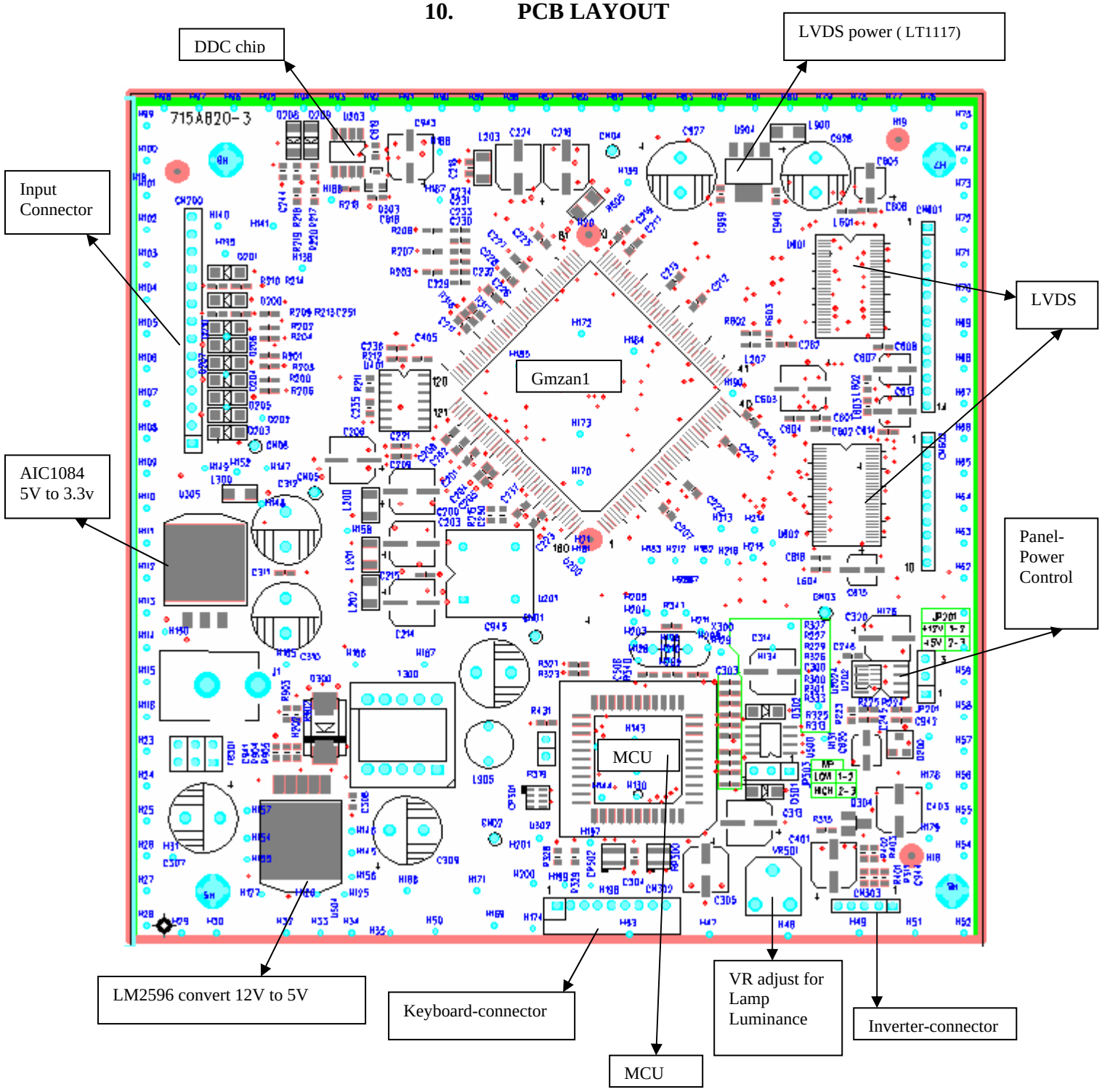
PARTS LIST OF AUDIO BOARD

LOCATION	AUPC780A1					Quantity	SPECIFICATION
P1	33A	3278	2			1	2P PLUG B2B-XHA/JST B2B-XHA/JS
P2	33A	3278	2			1	2P PLUG B2B-XHA/JST B2B-XHA/JS
	33A	8009	12E	H		2	2*6 PIN DUAL ROW RIGHT ANGLE
U1	56A	572	3			1	AN7522 BY PANASONIC
R1	61A	172	103	5	2T	1	10K OHM 5% 1/4W
R2	61A	172	103	5	2T	1	10K OHM 5% 1/4W
R3	61A	172	333	5	2T	1	33K OHM 5% 1/4W
R12	61A	172	681	5	2T	1	680 OHM 5% 1/4W
R4	61A	172	683	5	2T	1	68K OHM 5% 1/4W
R10	61A	153M	109	5	9	1	1 OHM +－ 5% 3W
R11	61A	153M	109	5	9	1	1 OHM +－ 5 % 3W
R7	61A	175L	134	5	2T	1	130K OHM 5% 1/2 W
R5	61A	175L	153	5	2T	1	15K OHM 5% 1/2W
R6	61A	175L	153	5	2T	1	15K OHM 5% 1/2 W
C8	67A	309	101	4		1	100uF+－20% 25V Matshushita
C1	67A	309	109	7		1	1uF +－20% 50V
C2	67A	309	109	7		1	1uF +－20% 50V
C4	67A	309	109	7		1	1uF +－20% 50V
C5	67A	309	109	7		1	1uF +－20% 50V
C3	67A	309	222	3		1	2200uF +－20% 16V
VR1	75A	347A	103	5	5G	1	VR 10K OHM 9mm 30/12
S1	77A	411A	2	S		1	PUSH SW PS02-BAN
D1	81A	2	3	2		1	LED LAMP-GREEN CSL-310G3GT
J2	88A	302	4S			1	3.5mm P JACK SCJ-0356A-B-X SC
	90A	400	1			1	HEAT SINK
J003	95A	90	23			0	TIN COATED
J004	95A	90	23			0	TIN COATED
	95A	8013	2	2	8	1	HARNESS 2P
	95A	8013	3	2	3	1	HARNESS 3P-2P
	M1A	330	6128			2	SCREW M3X6mm
	715A	799	1			1	17”LCD AUDIO BOARD 76.0 X 1

9. POWER SYSTEM AND CONSUMPTION CURRENT

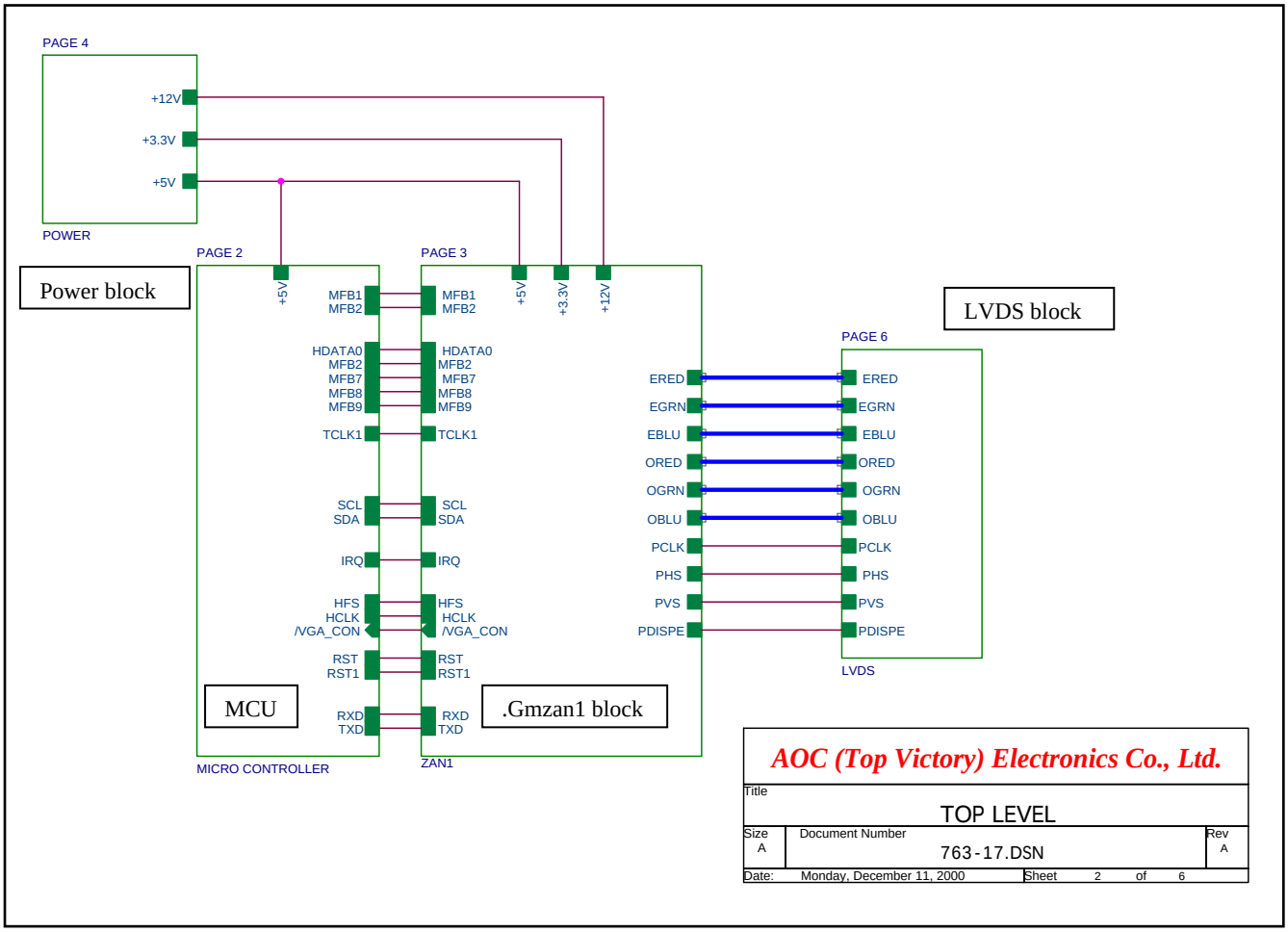


10. PCB LAYOUT

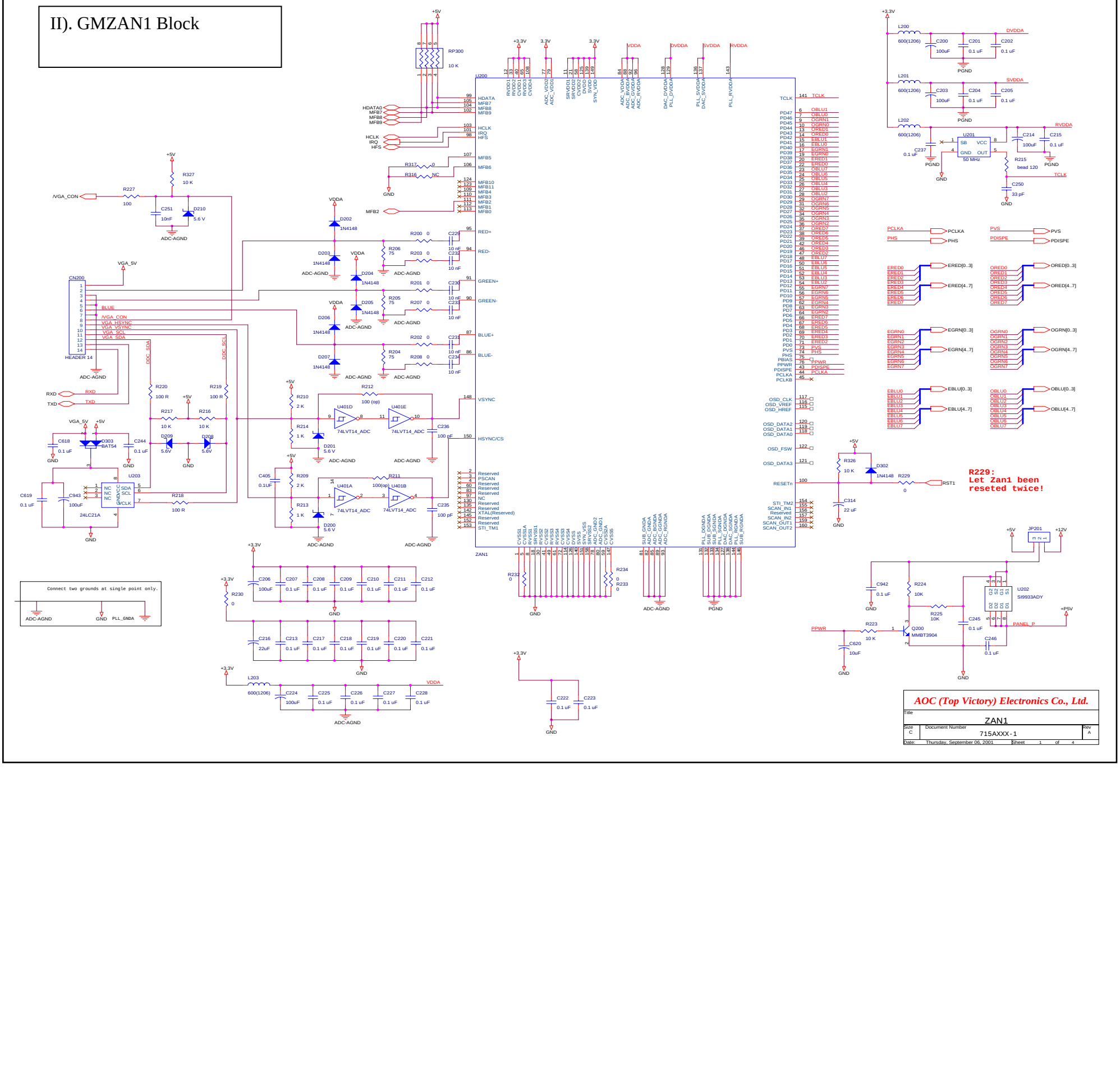


11. SCHEMATIC DIAGRAM

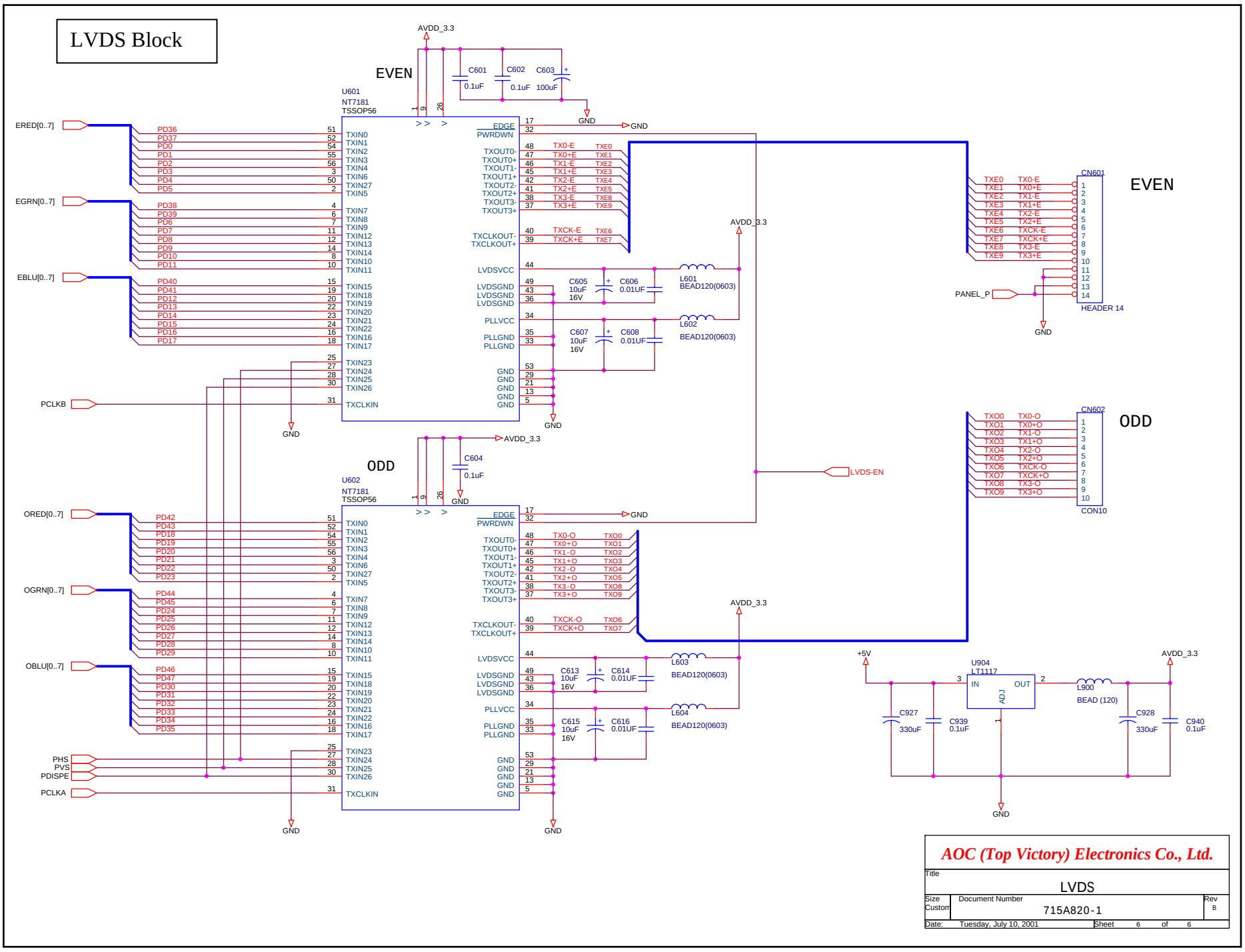
I). TOP-LEVEL FLOW



II). GMZAN1 Block



LVDS Block



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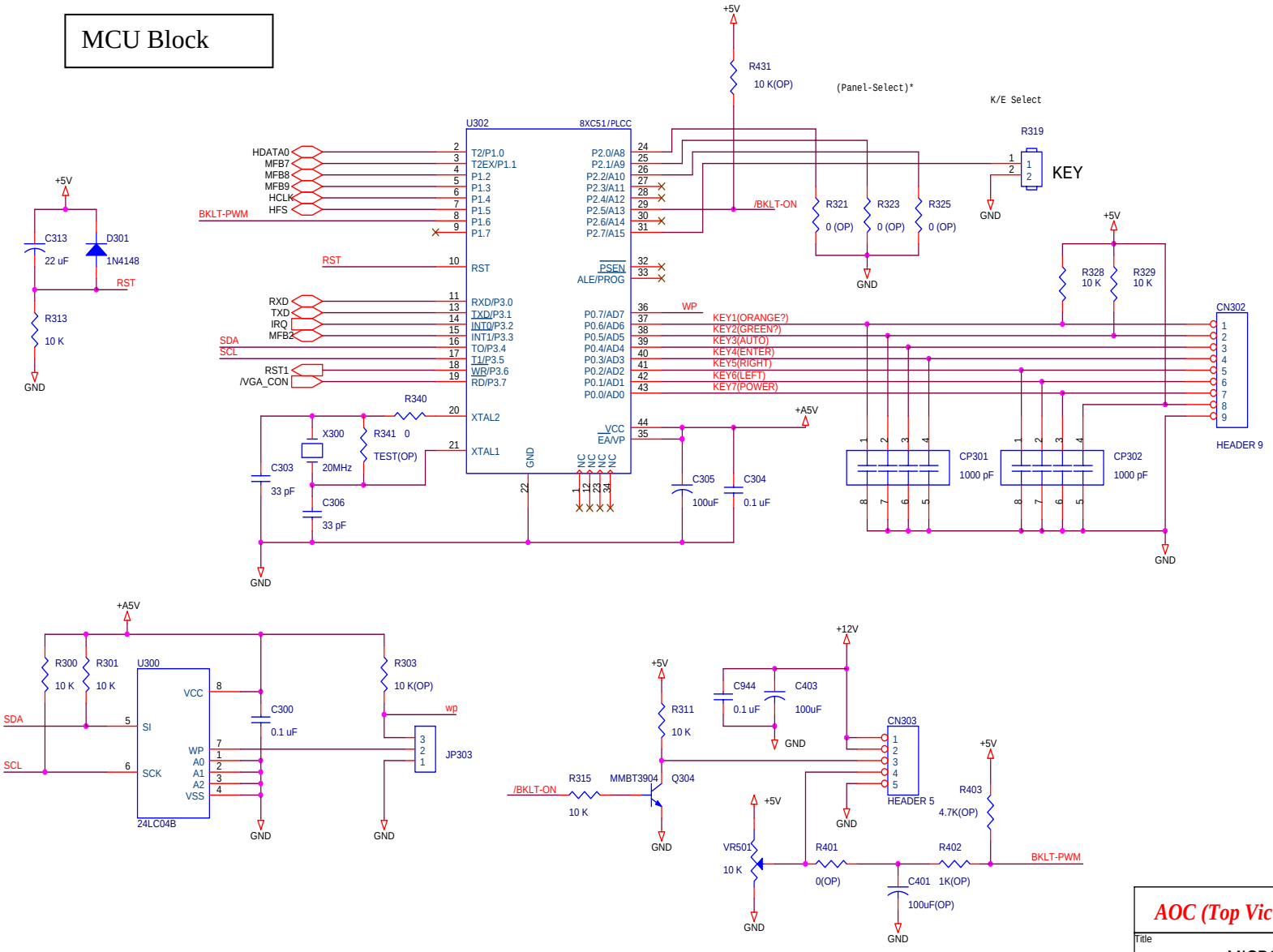
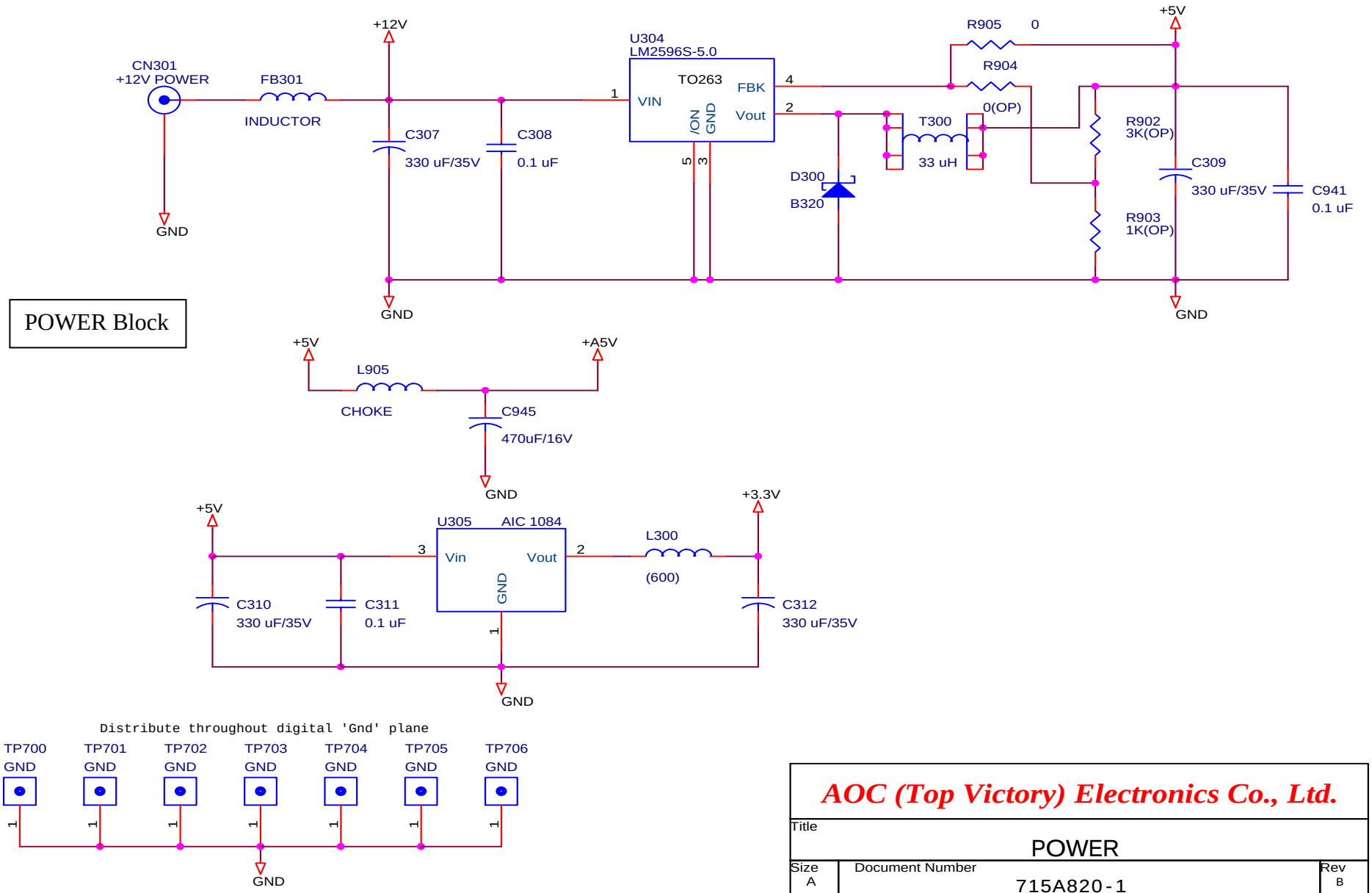
Title	LVDS	
Size: Custom	Document Number: 715A820-1	Rev: B
Date: Tuesday, July 10, 2001	Sheet 6 of 6	

MCU Block



AOC (Top Victory) Electronics Co., Ltd.		
Title: MICRO CONTROLLER		
Size: B	Document Number: 715A820-1	Rev: B
Date: Tuesday, July 10, 2001	Sheet 3 of 6	



AOC (Top Victory) Electronics Co., Ltd.		
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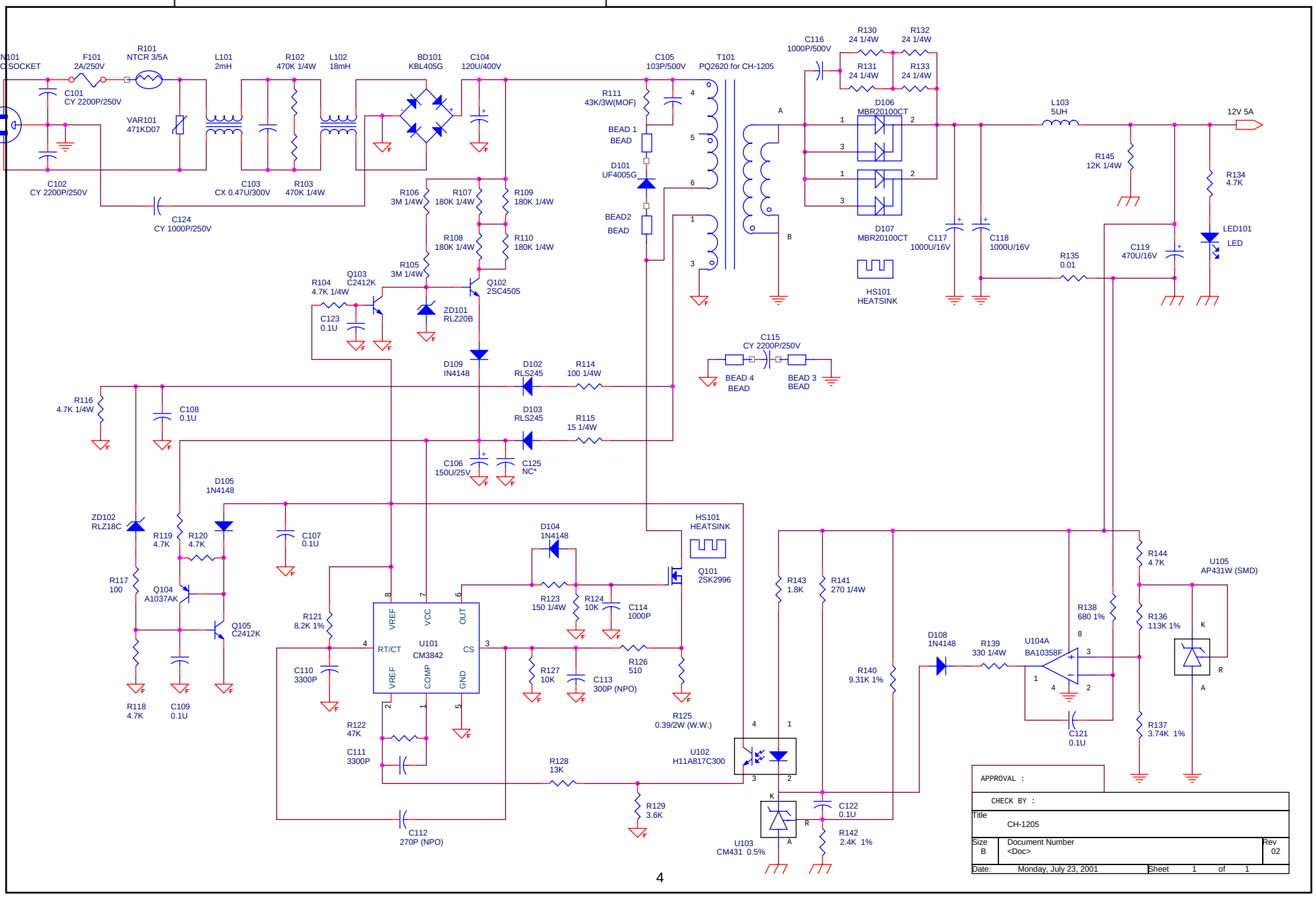
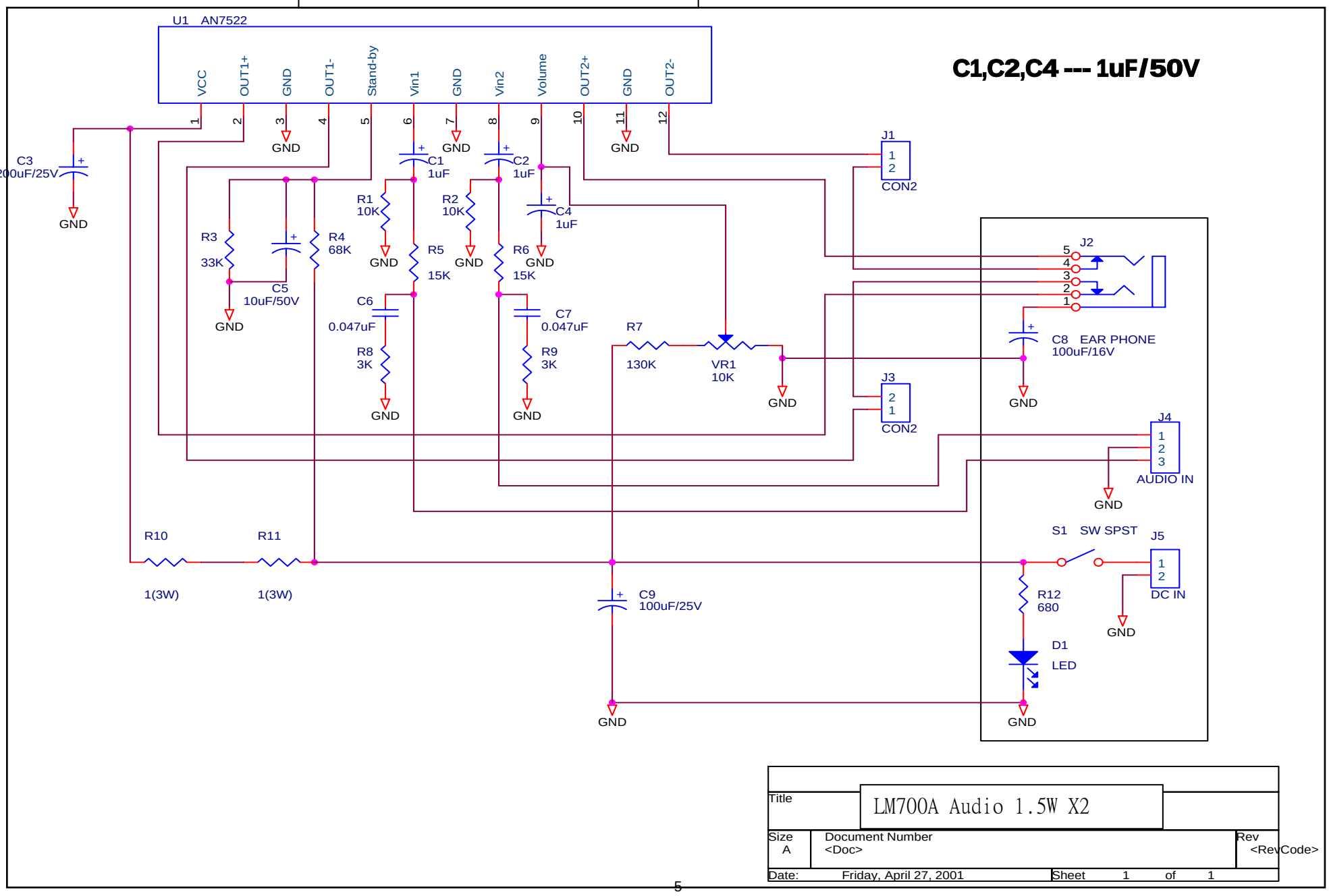
Size: A	Document Number: 715A820-1	Rev: B
Date: Tuesday, July 10, 2001	Sheet 5 of 6	

12.) ADAPTER SCHEMATIC CH-1205



13.AUDIO SCHEMATIC DIAGRAM



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Size A	Document Number <Doc>		Rev <RevCode>
Date: Friday, April 27, 2001		Sheet 1 of 1	